As the scaling of Si transistors is reaching its limit, they are expected to have new gate architectures, channel materials and switching mechanisms which have both high integration and low power consumption. Our tunnel FET is a next generation transistor exceeding the limit of Si transistors.

1. Epitaxial Growth of III-V Nanowire on Si
- Tunnel FET has not been achieved because narrow band gap III-V/Si is a highly mismatched system.
- Selective area growth brings epitaxial III-V nanowire on Si (111) substrate

2. Device Structure of Vertical Tunnel FET
- 30º-tilted view of SEM image
- Device schematic

3. High Performance of Vertical Tunnel FET
- The combination of a narrow band gap III-V with Si is a good system for boosting up the ON-state current and has high band-to-band tunneling efficiency.
- Very steep turn-on switching was observed. The subthreshold slope (SS) is far lower value than 60mV/dec.(theoretical limit value) of Si FET.

4. Patent available for licensing
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