JST-DFG workshop on NANOELECTRONICS

Self-Assembled Monolayers – Organic Electronics on the Molecular Scale

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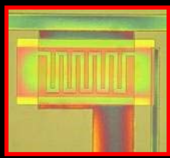
Outline

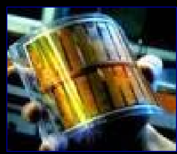
1. Motivation
2. The Platform – Organic Thin Film Transistors (TFTs)
   - Device Functionality
   - Interfaces
   - Molecules at Interfaces
3. Ultralow-Power Organic Electronics
   - Molecular Gate Dielectrics
   - Low-Power Complementary Circuits
   - Molecular Devices
4. Summary

Organic Electronics – Devices

thin film devices

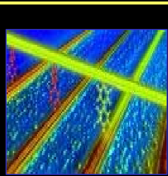

OLED


OFET (TFT)


solar cell


polymer memory

molecular devices


molecular memory

Trends in "Applications" of Organic Electronics

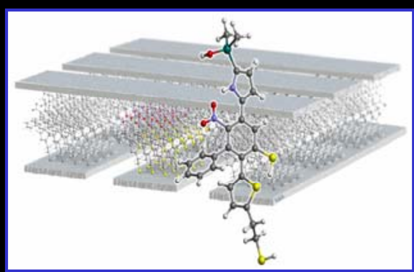
thin film electronics


Polymer Vision - Readius® (78.000 TFTs)

large feature size – flexible substrates
specialties - limited volume
large volume – low performance

supplementary products

molecular electronics



few nanometer feature size
(e.g. Green et al. *Nature* 445 414 (2007))

"next generation" products

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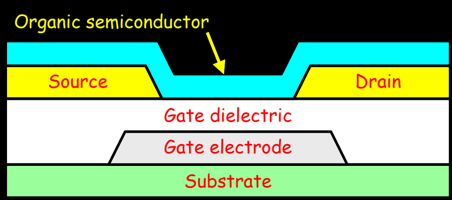
OTFT – Setup and Materials

- ***Semiconductor***
- S/D contact layer
- Gate dielectrics
- Gate electrode
- Substrate

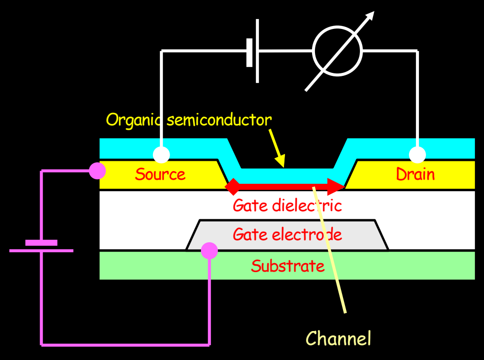


- Encapsulation
- OTFT architecture, …

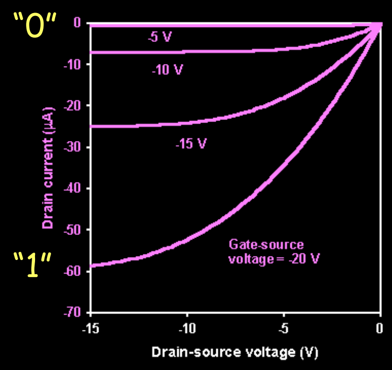
4 layer device
plus substrate

… polymers, small molecules, metals, ceramics !

What is an OTFT and How Does it Works?



electrical
output characteristics

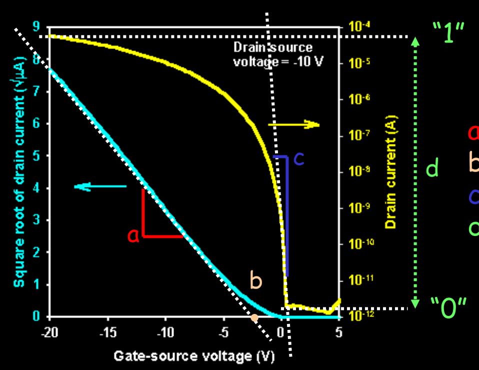


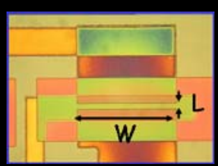
OTFT - electronic switch modulated by gate voltage
➔ digital "0" and "1" state

OTFT – Important Electrical Parameter

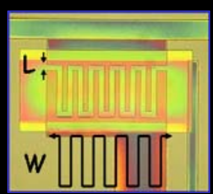
$$I_D = \frac{1}{2}\,\mu_{eff}\,C_i\,\frac{W}{L}\,(V_G - V_T)^2$$

transfer characteristics





W/L (100μm/10μm) = **10**



W/L (1000μm/10μm) = **100**

a) Carrier mobility μ = 0.5 cm²/Vs
b) Threshold Voltage V_{th} = -3 V
c) Subthreshold slope 0.2 V/decade
d) On/off current ratio 10^8

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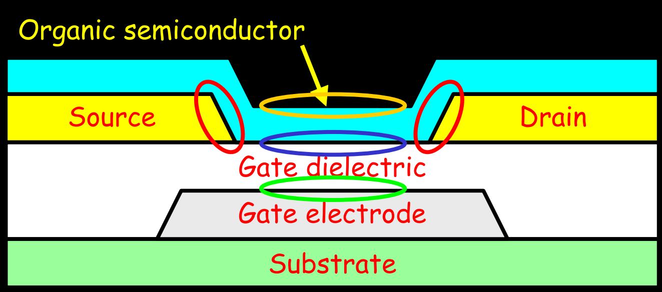
Interfaces – The Key in Device Performance



contact/semiconductor (charge injection/extraction)
dielectric/semiconductor (order, channel resistance)
control electrode/dielectric (order, roughness, capacity)
semiconductor/environment (stability, sensor properties)

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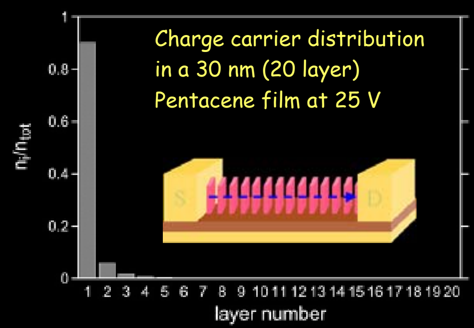
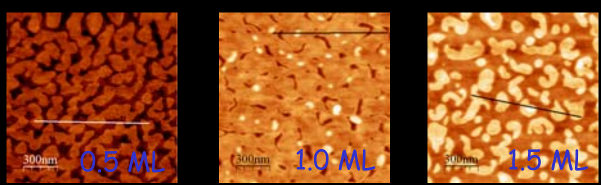
The Importance of the Interface



- > 90% of charge is carried in the first monolayer
- "quality" of 1st ML is dominated by surface (dielectric layer)
- grain size (lattice size) is only a crude indication for large μ



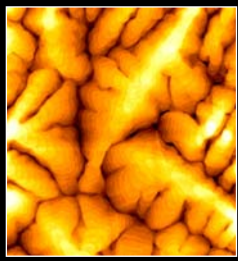
no FE | 0.05 cm²/Vs | 0.25 cm²/Vs

Oligothiophenes

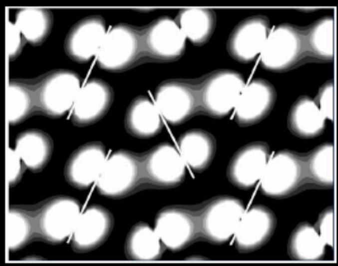
Horowitz et al. *Org. Electronics*, 7, 528 (2006)
Halik et al. Org. Electronics, 9, 1061 (2008)

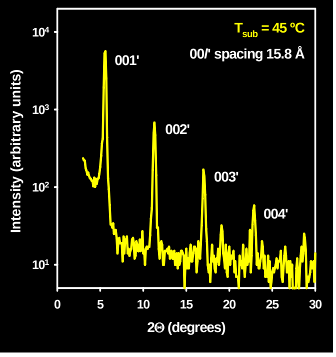
Organic Semiconductors: Pentacene

- tendency to form <u>molecular crystals</u> perpendicular to surface.
- micron-size grains with terracing
- efficient $\pi\pi$-interaction



Homo electron density, looking along c-axis
(K. Hummer, P. Puschnig, C. Ambrosch-Draxl *Electronic Properties of Oligo-Acenes*, April 2003, Vienna, Austria)

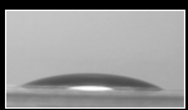


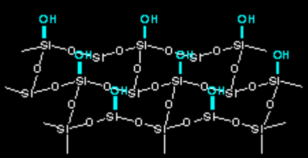


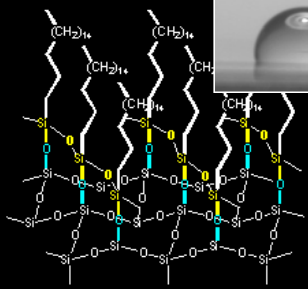
Gundlach et al., *IEEE Electr. Dev. Lett.* 18, 87 (1997)
D. Knipp et al., *J. Appl. Phys.* 93, 347 (2003)

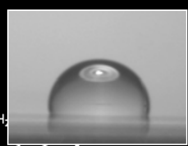
The Self-Assembly Process

<u>substrate</u>: serving a suitable surface for anchor group (e.g. Si-OH or Al-OH)
<u>molecule</u>: reactive anchor group (e.g. SiR_3; R= Cl, OEt) and "right shaped" molecule
<u>deposition</u>: dip casting from solution or MVD (molecular vapor deposition)







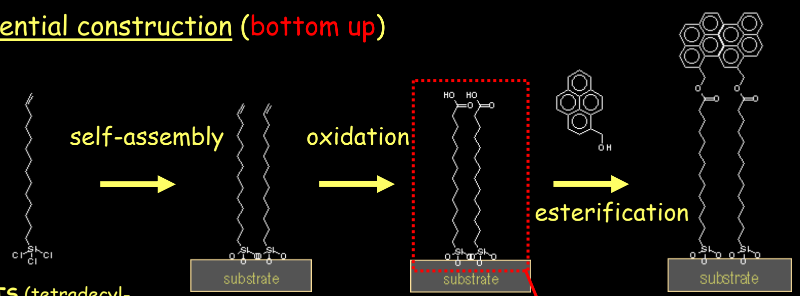


bare silicon wafer
(substrate and gate electrode)
natively oxidized or briefly activated
(O_2-plasma treatment)
static contact angle (H_2O) ∠ 10°

organic molecular layer
(e.g. OTS)
covalently bond on surface
static contact angle (H_2O) ∠ 100°

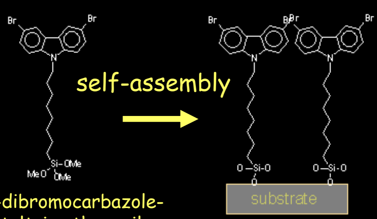
Approaches in SAM Preparation

sequential construction (bottom up)



TETS (tetradecyl-1-enyltrichlorosilane)

direct grafting (top down)

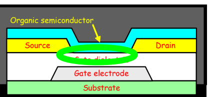


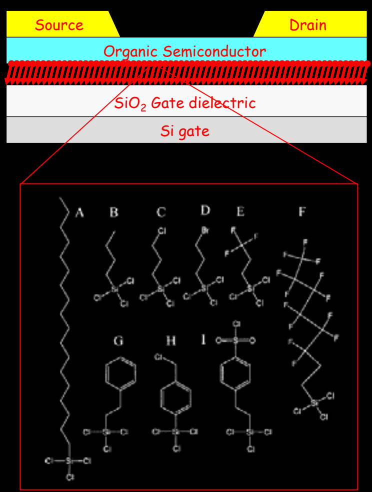
3,6-dibromocarbazole-N-octyltrimethoxysilane

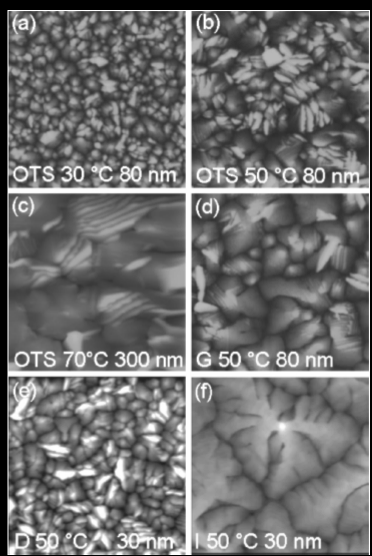
pioneering work on SAM dielectric TFTs

Collet et al. *Appl. Phys. Lett.*, 73, 2681 (1998); 76, 1339 (2000); 76, 1941 (2000)

Dielectric Surface Treatment







SAM impacts on molecular order of thin film organic semiconductor

Pernstich et al. JAP 96, 6431 (2004)

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2. The Platform – Organic Thin Film Transistors (TFTs)
    - Device Functionality
    - Organic Semiconductor Materials
    - Integrated Circuits
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Why "Ultralow-Power" ????

power saving – a social convention in today!!!

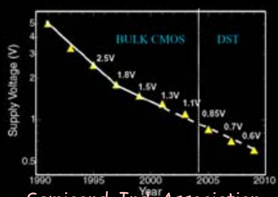
- portable devices powered by
  - small batteries
  - near-field frequency coupling

PolyIC

Someya et al.
Nat. Mater. 6, 413, (2007)

- interaction with Si world
  - controller ICs

Plastic Logic



Semicond. Ind. Association

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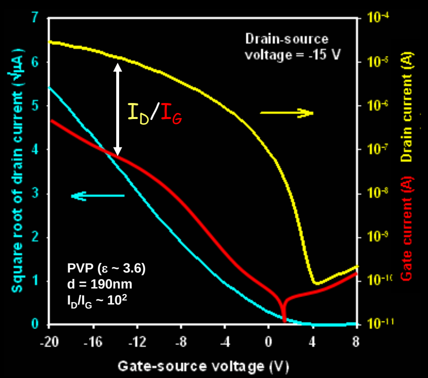
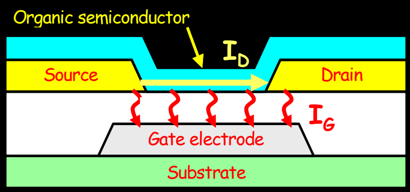
Operating Voltage Problem



$$I_D = \frac{1}{2}\mu_{eff}\, C_i \frac{W}{L}(V_G - V_T)^2$$

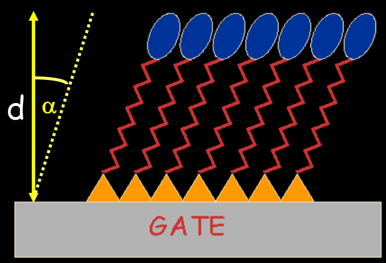
$$C_i = \varepsilon_0 \varepsilon \frac{A}{d}$$

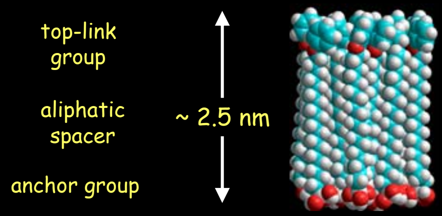
high ε or small d



"Traditional" low-temperature gate dielectrics (CVD-SiO_2, SiN_x, polymers) must be at least 50 nm thick to reduce gate leakage (I_G).
This leads to supply voltages too large for most applications (up to 100V).

The Approach: Self-Assembled Monolayers



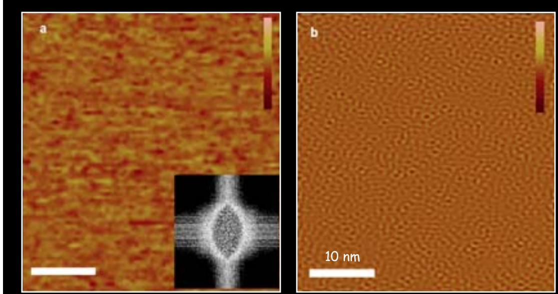


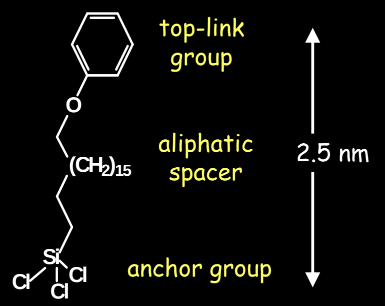
Requirements:

1. large area coverage without pinholes to prevent electrical shorts
2. dense packaging and sufficient length to prevent leakage
3. chemically and thermally stable to realize integrated devices

Dense Molecular Self-Assembled Monolayers

STM image:
(raw data) (band-pass filtered)

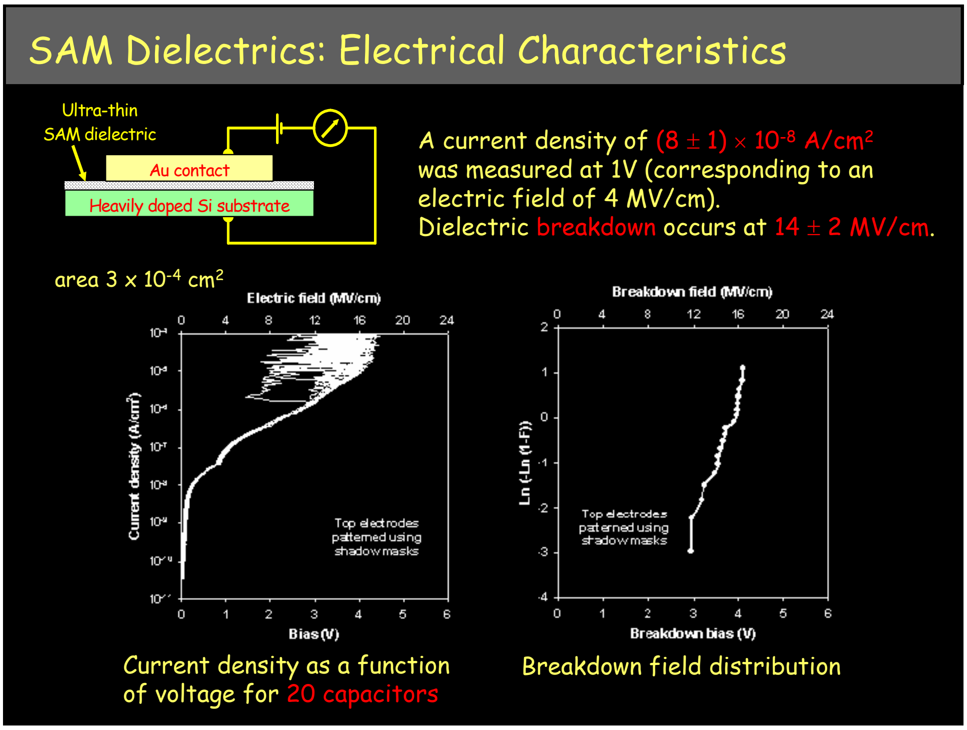


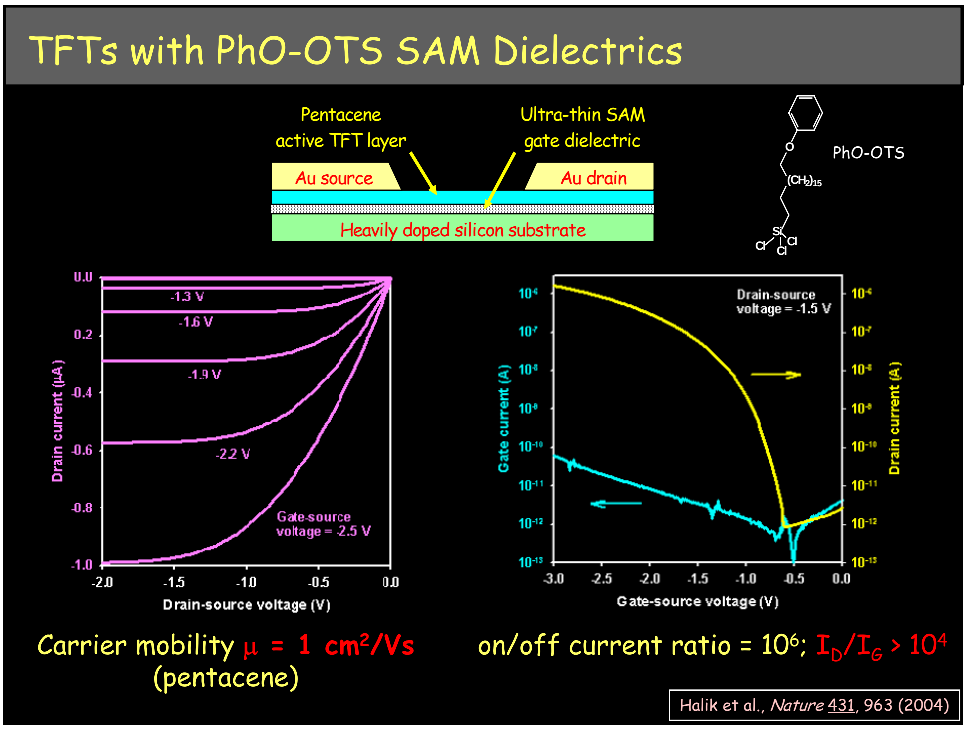


Molecular self-assembled monolayers with benzene "top-link" are perfectly amorphous (without grain boundaries) and free of defects over large areas (many square microns).

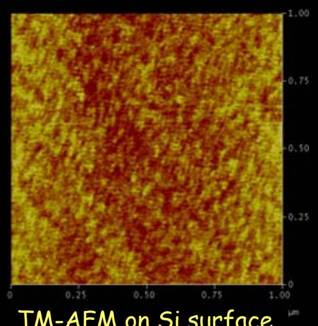
PhO-OTS
(18-phenoxyoctadecyl) trichlorosilane

Halik et al., *Nature* 431, 963 (2004)

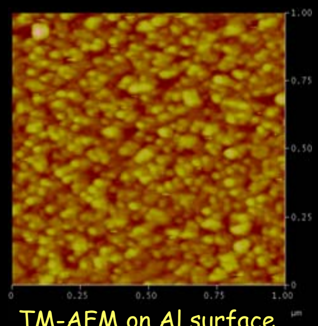

SAM Dielectrics: Electrical Characteristics
Ultra-thin SAM dielectric
Au contact
Heavily doped Si substrate
area 3 x 10-4 cm2
A current density of (8 ± 1) × 10-8 A/cm2 was measured at 1V (corresponding to an electric field of 4 MV/cm).
Dielectric breakdown occurs at 14 ± 2 MV/cm.
Electric field (MV/cm)
Current density (A/cm²)
Top electrodes patterned using shadow masks
Bias (V)
Breakdown field (MV/cm)
Ln (-Ln (1-F))
Breakdown bias (V)
Current density as a function of voltage for 20 capacitors
Breakdown field distribution


TFTs with PhO-OTS SAM Dielectrics
Pentacene active TFT layer
Ultra-thin SAM gate dielectric
Au source
Au drain
Heavily doped silicon substrate
PhO-OTS
Drain current (µA)
Drain-source voltage (V)
Gate-source voltage = -2.5 V
-1.3 V
-1.6 V
-1.9 V
-2.2 V
Gate current (A)
Drain current (A)
Drain-source voltage = -1.5 V
Gate-source voltage (V)
Carrier mobility µ = 1 cm²/Vs (pentacene)
on/off current ratio = 10⁶; I_D/I_G > 10⁴
Halik et al., Nature 431, 963 (2004)

From Single Crystalline Silicon to Metal Surfaces

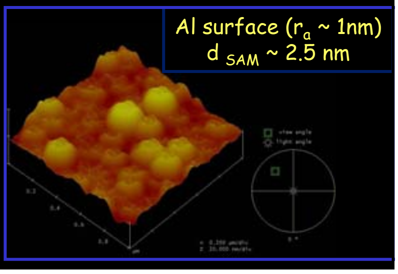


TM-AFM on Si surface

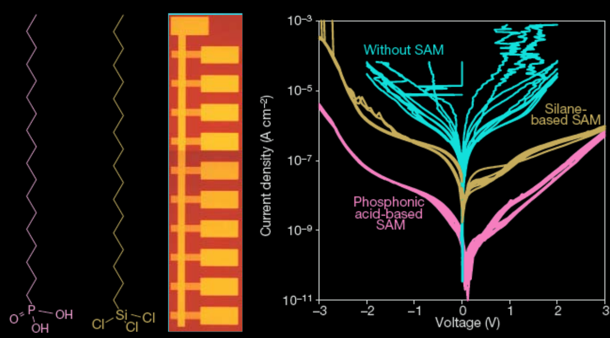


TM-AFM on Al surface

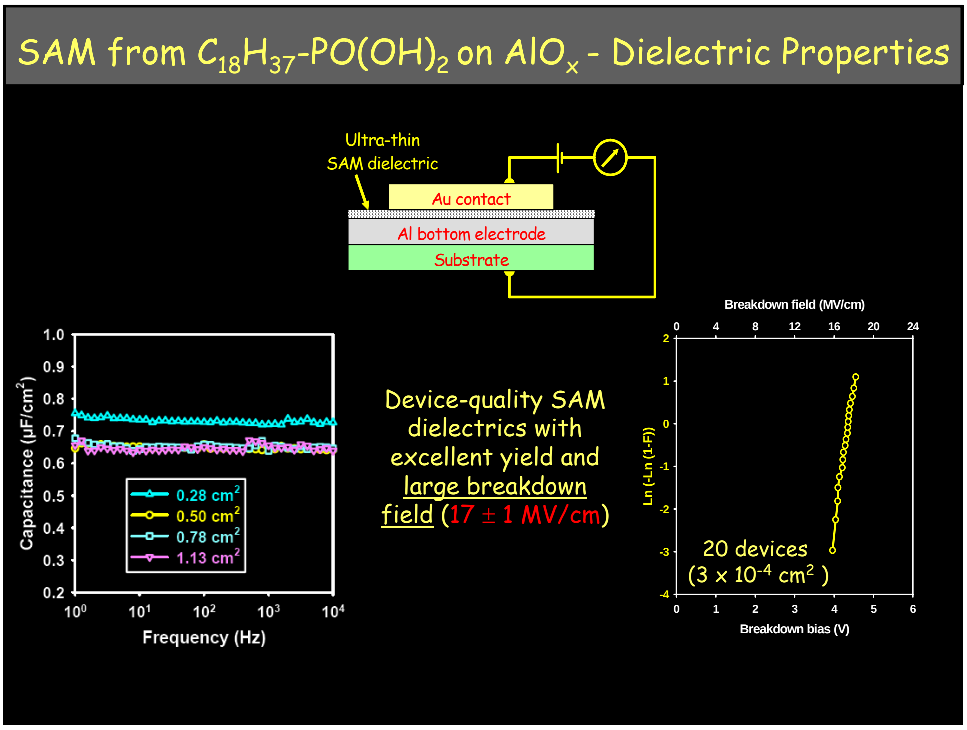
During the Si surface is "ideal" flat (« 1nm) the Al sample shows a rough surface (~ 1nm). However Si and Al serve a reactive surface for self-assembling (native or plasma treated).

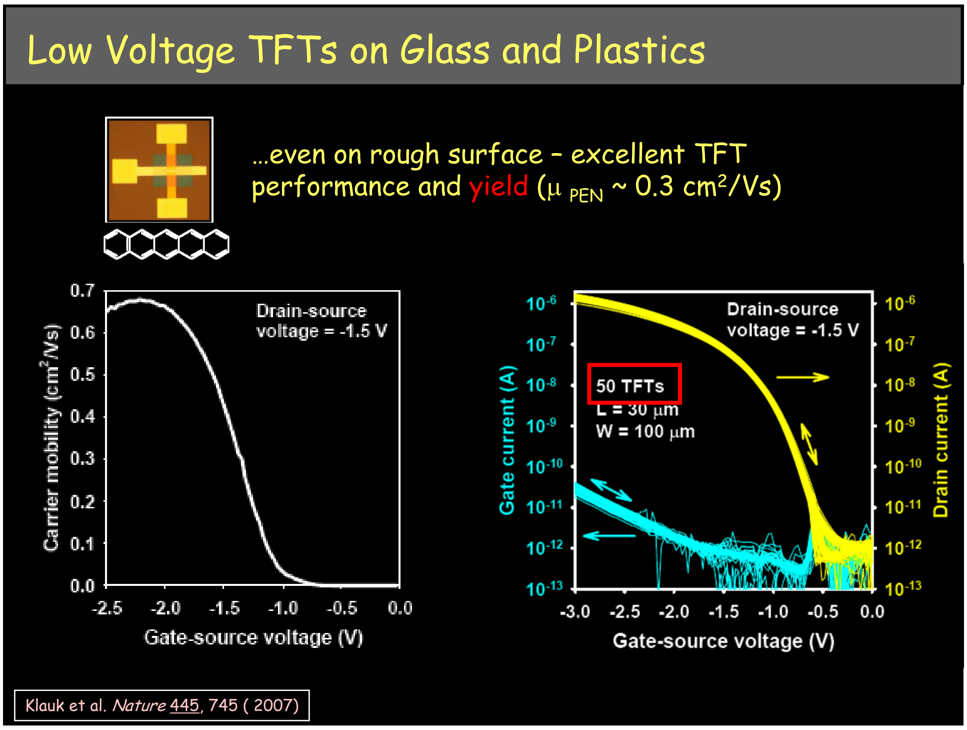


SAMs with Phosphonic Acid Anchor Group

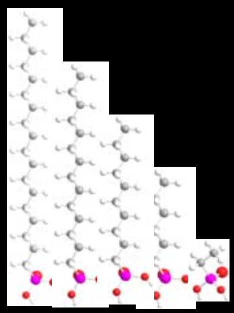


Density of packaging is 2.5 times larger for phosphonic acid based SAM compared to silane based SAM (calculated from XPS data)

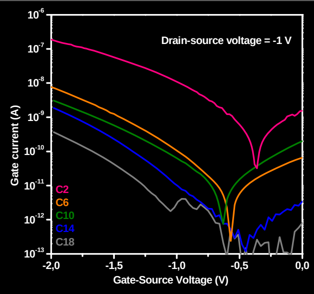

SAM from $C_{18}H_{37}$-PO(OH)$_2$ on AlO$_x$ - Dielectric Properties
Ultra-thin SAM dielectric
Au contact
Al bottom electrode
Substrate
Capacitance (µF/cm²)
Frequency (Hz)
0.28 cm²
0.50 cm²
0.78 cm²
1.13 cm²
Device-quality SAM dielectrics with excellent yield and large breakdown field (17 ± 1 MV/cm)
Breakdown field (MV/cm)
Ln (-Ln (1-F))
20 devices
(3 x 10^{-4} cm²)
Breakdown bias (V)


Low Voltage TFTs on Glass and Plastics
…even on rough surface - excellent TFT performance and yield (μ_{PEN} ~ 0.3 cm²/Vs)
Carrier mobility (cm²/Vs)
Drain-source voltage = -1.5 V
Gate-source voltage (V)
Gate current (A)
Drain current (A)
50 TFTs
L = 30 µm
W = 100 µm
Klauk et al. Nature 445, 745 (2007)

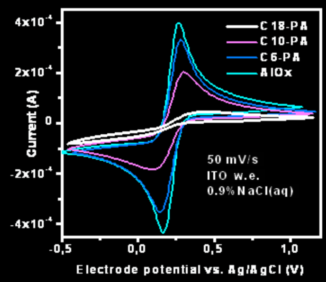
Sub-nanometer Changes in Molecular Dielectric Thickness



2.5 nm – 0.5nm



TFT gate leakage related to sub-nm changing in SAM dielectric thickness (40 x 100 μm area)



CV-characteristics independent method (electrode area ~ 5 cm²)

Burkhardt et al. Org.Electr. Workshop (2008), Halik et al. submitted to Small

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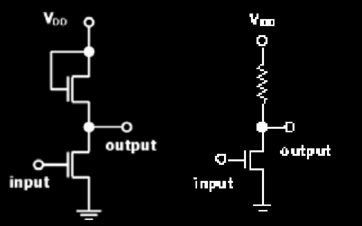
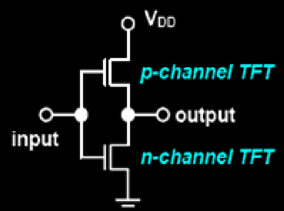
The Advantage of Complementary Circuits

single carrier type
(p- or n-type)
saturated (resistive) load

two carrier types
(p- and n-type)
complementary device



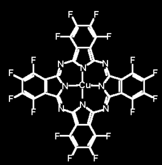


large static power dissipation
one transistor is "slightly in conductive "on-state"

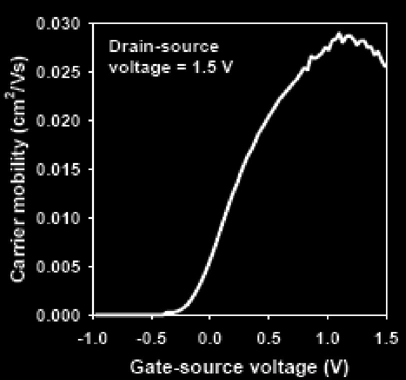
very low static power dissipation
all transistors are in non-conducting "off-state" – except during switching (idling)

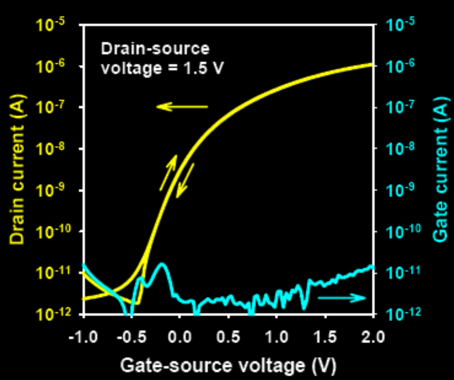
!! need for high performance n-type organic semiconductors !!

Low Voltage TFTs with $F_{16}CuPc$ (n-type)



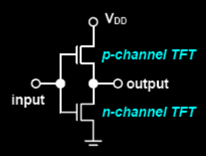
…slightly reduced electron mobility
compared to hole mobility of pentacene
(measured in ambient)



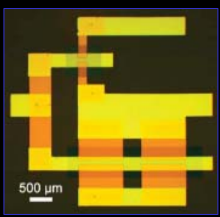


"CMOS-like" Ultra Low Power Circuits

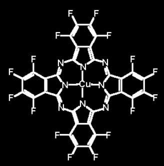
…fabricated without lithography and at low temperatures (max. 90°C)



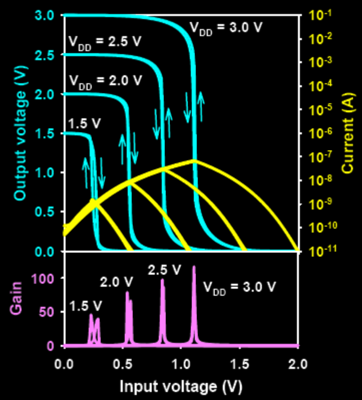
inverter



μ PENTACENE ~ 0.7 cm²/Vs



μ F16CuPc ~ 0.03 cm²/Vs

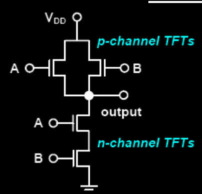


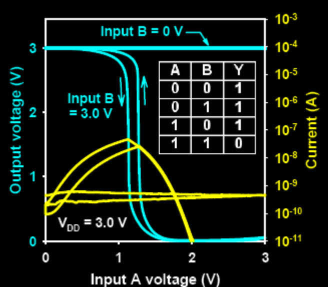
excellent gain (> 100)
negligible static power consumption
(less than 1 nW per logic gate)

Klauk et al. *Nature* 445, 745 (2007)

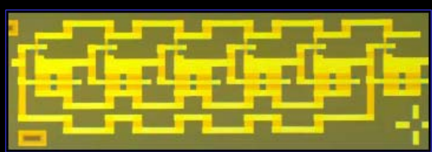
"CMOS-like" Ultra Low Power Circuits

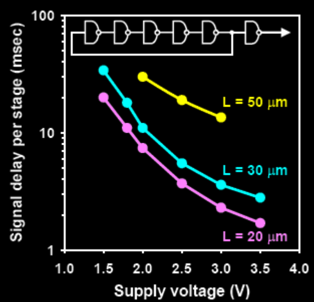
NAND gate





ring oscillator



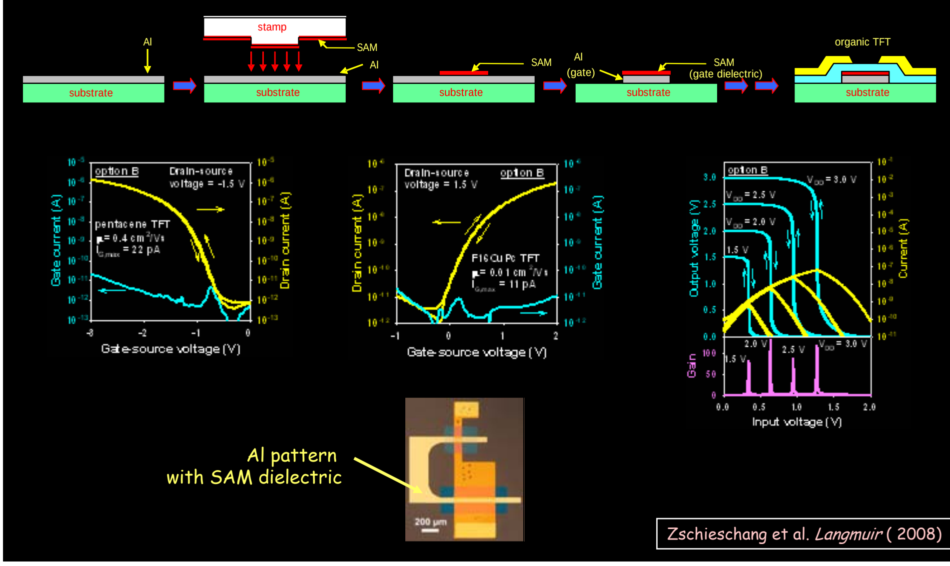


circuit speed scales with L
and supply voltage

Klauk et al. *Nature* 445, 745 (2007)

Printed SAM Dielectrics

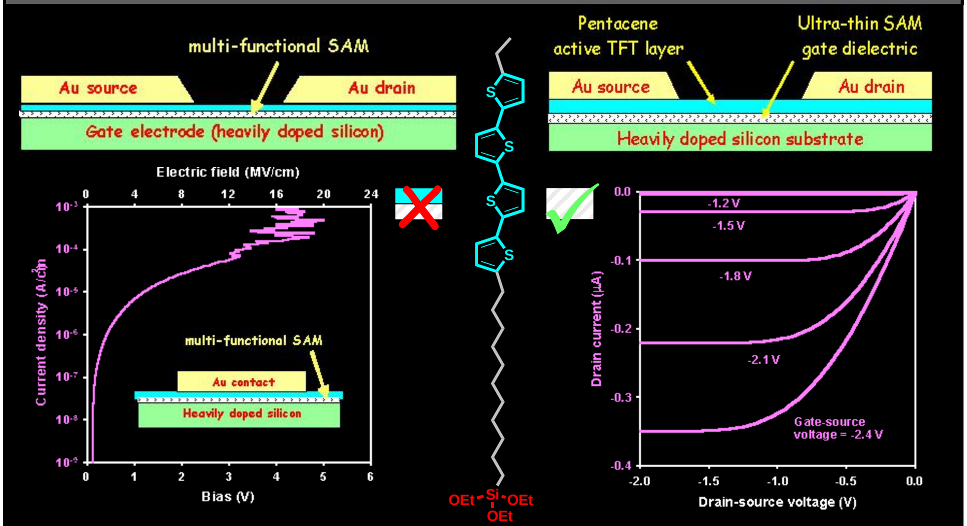
SAMs are suitable for patterning Al and serving dielectric layer in one step



Zschieschang et al. *Langmuir* (2008)

1. Motivation
2. The Platform – Organic Thin Film Transistors (TFTs)
   - Device Functionality
   - Interfaces
   - Molecules at Interfaces
3. Ultralow-Power Organic Electronics
   - Molecular Gate Dielectrics
   - Low-Power Complementary Circuits
   - Molecular Devices
4. Summary

The Dream – Towards "Molecular Transistor" ☹ 2006



- SAM as multi-functional molecule (anchor, dielectric and semiconductor)
- Behaves as insulator – limited by anisotropic charge transport of 4T
- with Pentacene - TFTs show excellent low-voltage performance (μ = 0.5 cm²/Vs)

Summary

Molecular layers have impact on all interfaces and can improve device performance

Molecular layers can act as active device layer with:
excellent, reliable and robust dielectric properties
- on different electrode materials
- on large areas and even flexible substrates and
- for various organic semiconductors

…to make "Ultralow-Power Organic Electronics" possible
…and to realize molecular scale electronics!!!!!

Multi-functional layers provide molecular TFT properties

... the People Involved:

Martin Burkhardt, Abdesselam Jedaa, Michael Novak, Hendrik Faber, Dana Salewsky
OMD Group University Erlangen-Nuernberg

Hagen Klauk*, Ute Zschieschang*, Florian Eder ‡, Günter Schmid‡
Infineon Technologies, Materials & Technology, Erlangen
* now at MPI for Solid State Research Stuttgart
‡ now at SIEMENS AG, CT MM1

Sergei Ponomarenko, Timo Meyer-Friedrichsen, Stephan Kirchmeyer
H.C. Starck / Bayer AG, Leverkusen

Markus Schütz, Steffen Maisch, Franz Effenberger
University Stuttgart, Department of Chemistry

Markus Brunnbauer, Francesco Stellacci
Massachusetts Institute of Technology, Department of Materials Science and Engineering

Andreas Hirsch, Alexander Ebel
OC II University Erlangen

Thank you for attention !

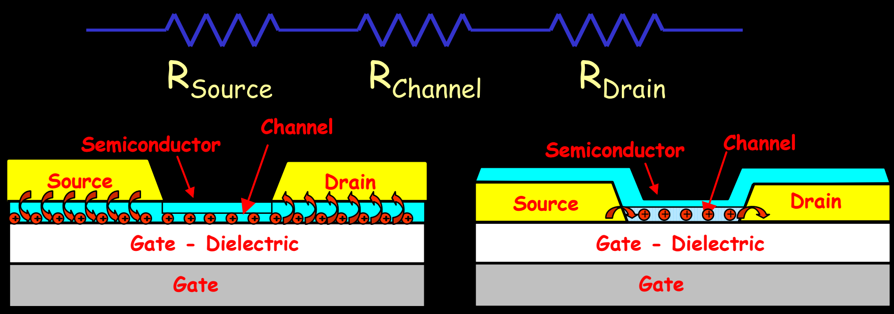
http://www.omd.uni-erlangen.de

.....€€€€€€ ....

Cluster of Excellence –
Engineering of Advanced Materials

Deutsche Froschungsgemeinschaft - DFG

Contact Resistance vs. Channel Resistance



Charge injection (contact resistance) dominates the TFT performance!

$$I_D = \frac{V_{DS}}{R_{source} + R_{channel} + R_{drain}}$$

example - bottom contact TFT

- minimum contact resistance ($V_{GS} = V_{DS} = -10$ V): 4 MΩ
- contact resistance 5 .. 10 times larger than channel resistance (for L = 10 μm)

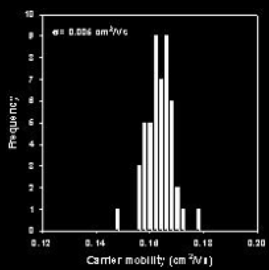
Klauk et al., *Solid-State Electr.* 47, 297 (2003)

1. Motivation
2. The Platform – Organic Thin Film Transistors (TFTs)
   - Device Functionality
   - Organic Semiconductor Materials
   - Integrated Circuits
3. Ultralow-Power Organic Electronics
   - Molecular Gate Dielectrics
   - Low-Power Complementary Circuits
4. Summary

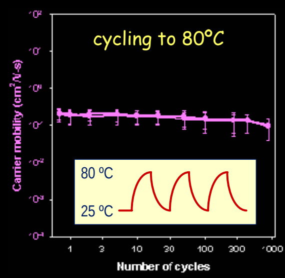
Performance of Pentacene TFTs and ICs

If all the issues related to materials and processing are addressed, a suitable device performance is expected.

- TFT yield > 98%
- statistical distribution of OTFT parameters (± 3%)
- environmental stability (> 80°C, > 70% humidity, etc.)
- shelf-life (> 1 year in ambient)
- dynamic endurance (> 10^7 switching cycles)



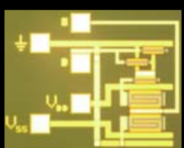
distribution - μ
(49 TFTs)



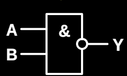
Halik et al. *E-MRS Spring Meeting* (2004)

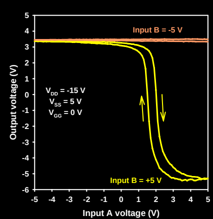
Integrated Circuits Based on OTFTs (p-channel)

NAND
(with level shift)



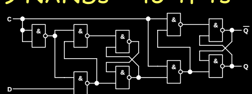
5 TFTs

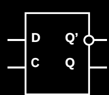




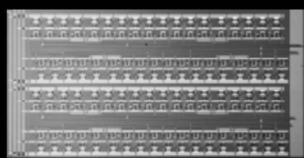
D flip flop
(divide-by-2)

9 NANDs = 45 TFTs

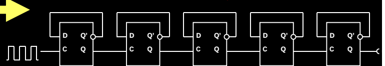




5-stage frequency divider
(divide-by-32)

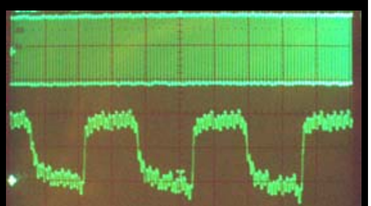


225 TFTs



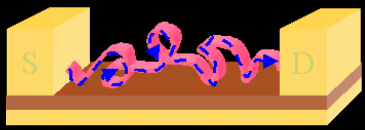
input signal

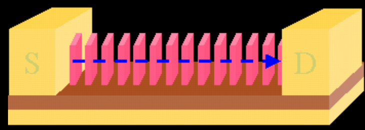
output signal



Lackner et al., *Int. Electr. Dev. Meet.* (2005)

Organic Semiconductors - Polymers / Small Molecules





- charge transport along chain and by inter-chain hopping (lattice)
- deposition from solution (pot. printing)
- low performance (0.01 – 0.3 cm²/Vs)
- relatively poor stability

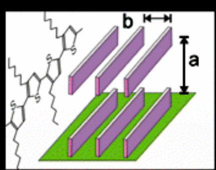
- charge transport through $\pi\pi$-stacking overlap
- deposition from vapor phase or solution
- high performance (0.1 – 3 cm²/Vs)
- reasonable stability

Poly-3-hexylthiophene
(regio-regular)

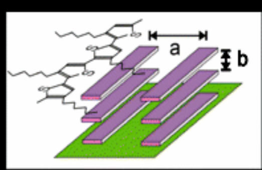
Pentacene
(twice sublimed)

Organic Semiconductors: Poly-3-hexylthiophene P3HT

Lattice orientation dominates the polymer performance
Performance is limited by semi-crystalline behavior



μ = 0.1 cm²/Vs

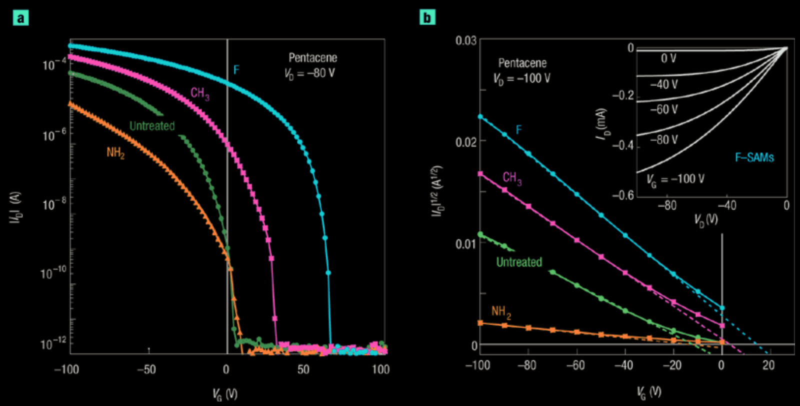


μ = 0.0002 cm²/Vs

Orientation depends on:
- surface (treatment)
- temperature
- deposition method, …

Sirringhaus et al. *Nature* 401, 685 (1999)

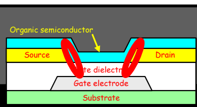
Interface Treatment – Electrical Impact



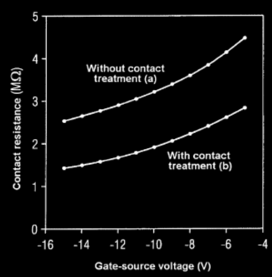
- molecular structure (dipole moment) affects transistor function (V_{th}; μ)
- demonstrated for several organic semiconductors (Pentacene, C60, Rubrene)

Kobayashi et al. Nat. Mater. (2004)
Pernstich et al. JAP 96, 6431 (2004)

Contact Treatment

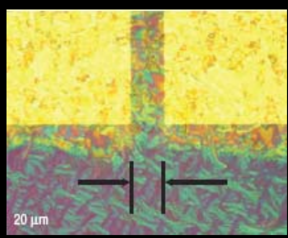


<u>modified contact properties</u>

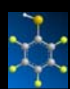


- reduced contact resistance
- optimized systems
  (Au/-SH; Pd/-CN; ITO/-PO(OH)$_2$ ...)
- selective grow (dip coating)

<u>tuned semiconductor properties</u>



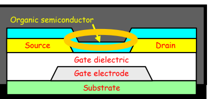
- induced crystal grow
- extended and oriented π-stacking
  (FF interaction)

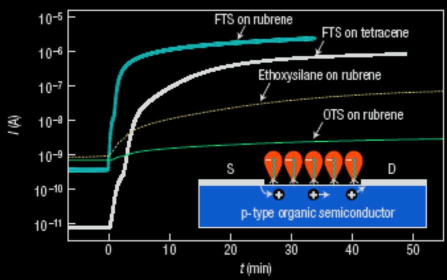


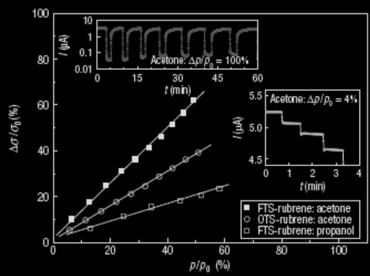
Halik et al. DE 102 34 997 C1; US 7,151,275 B2

Gundlach et al. *Nature Materials* (2008)

Semiconductor Treatment





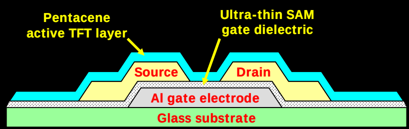


- semiconductor surface coating
- dipole impact on TFT channel
- increased I_d vs. time

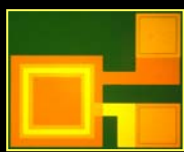
- SAM coating impacts on interaction with environment
- "sensor" application

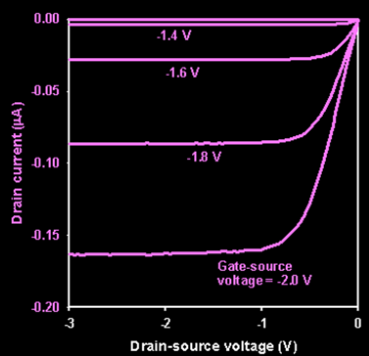
Calhoun et al. *Nature Materials* (2007)

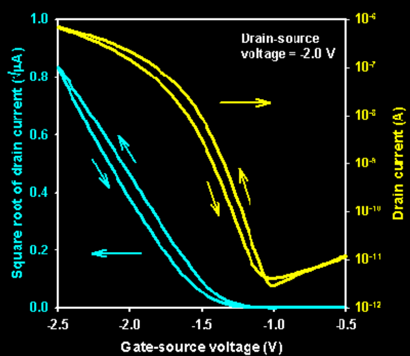
TFTs on Glass Substrates with Photolithographically Patterned Contacts



Corbino TFT:
Channel length/width
30 / 300 μm







Carrier mobility = 0.15 cm²/Vs
Threshold voltage = -1.4 V

Subthreshold slope = 110 mV/dec
on / off current ratio = 10^5

M. Halik, *Proc. SPIE* 5940 59400W (2005)