

# Scanning probe lithography on semiconductor heterostructures: Technology and scientific applications

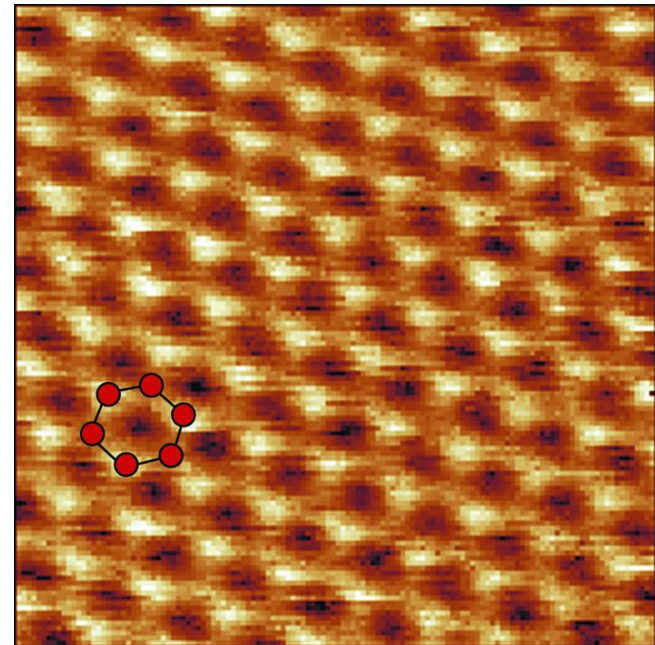
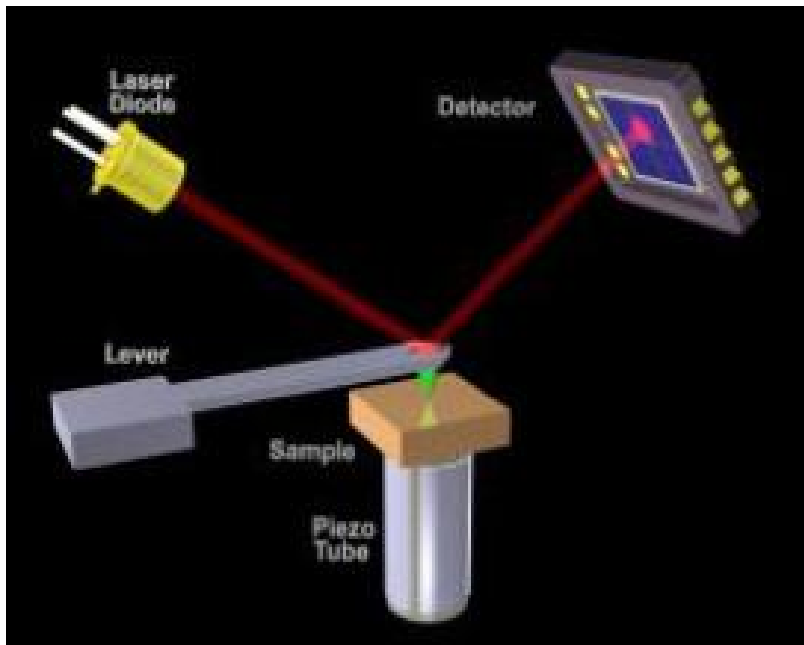
**Thomas Heinzel**

**Heinrich-Heine-Universität Düsseldorf**

- Motivation and technology
- Options offered
- Some application examples

## Why patterning with an AFM?

AFM image  
of a graphite surface

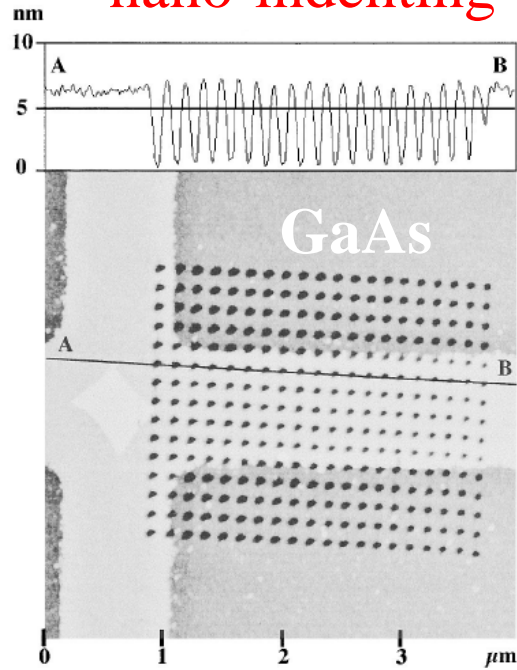


Figures: courtesy of the  
Swiss Nanoscience Institute (SNI)

➔ **Functional** modification of surfaces by AFMs?

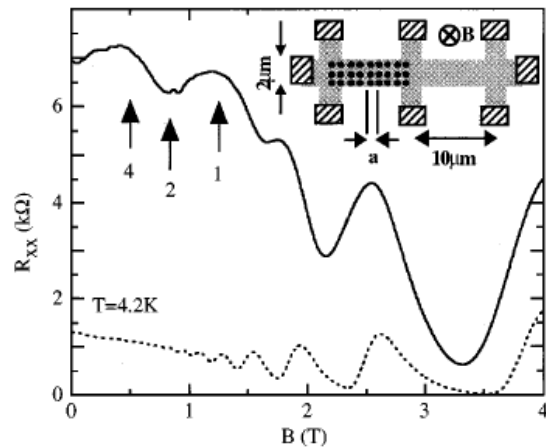
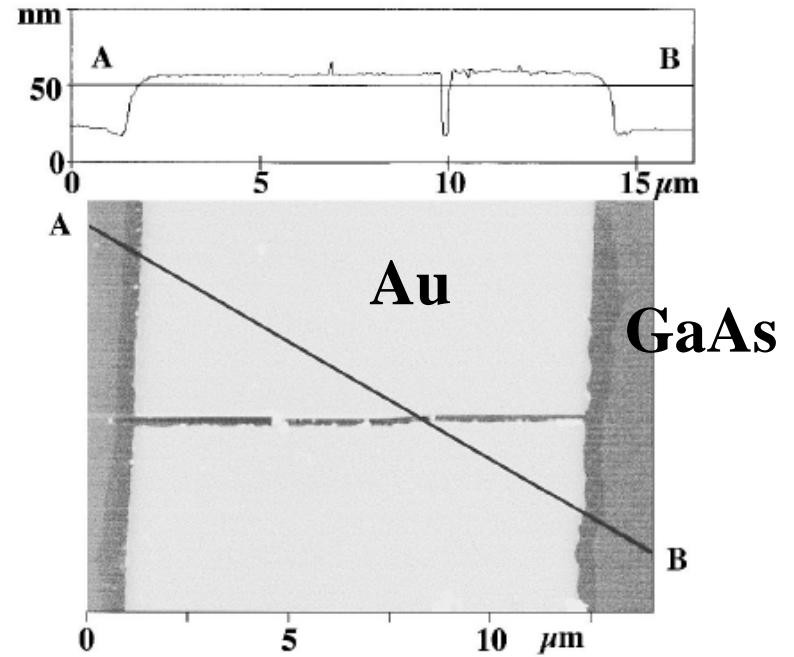
# The AFM as a mechanical tool:

nano-indenting



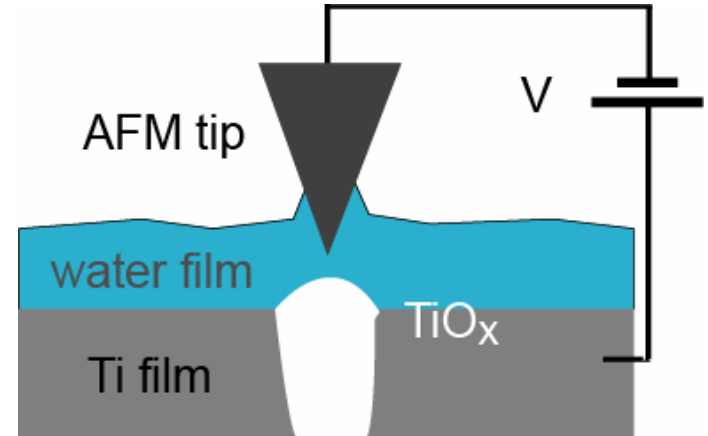
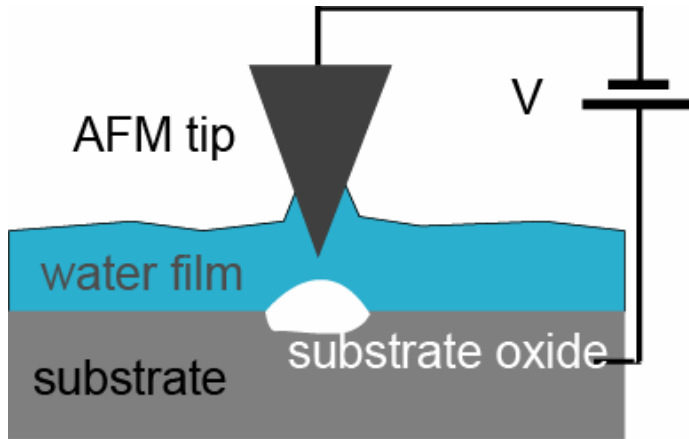
and

-plowing



M. Wendel et al., Appl. Phys. Lett. **65**, 1775 (1994)

# The AFM as an electrochemical tool: Local Oxidation



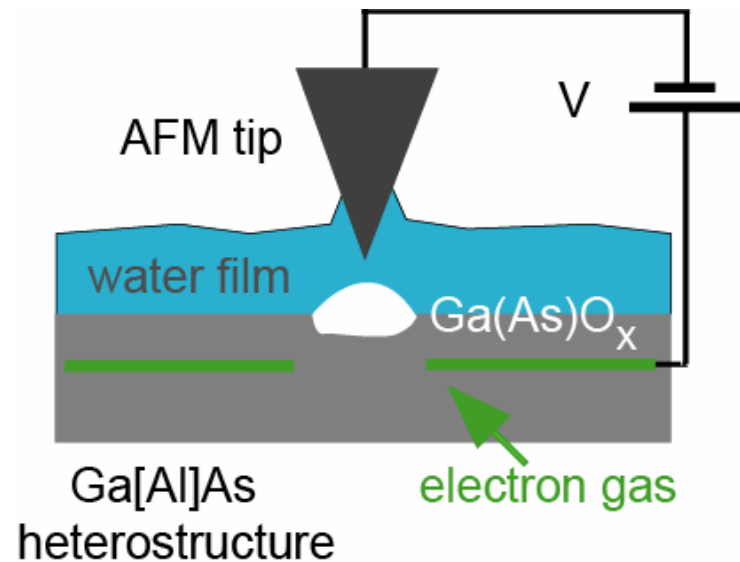
possible reaction:

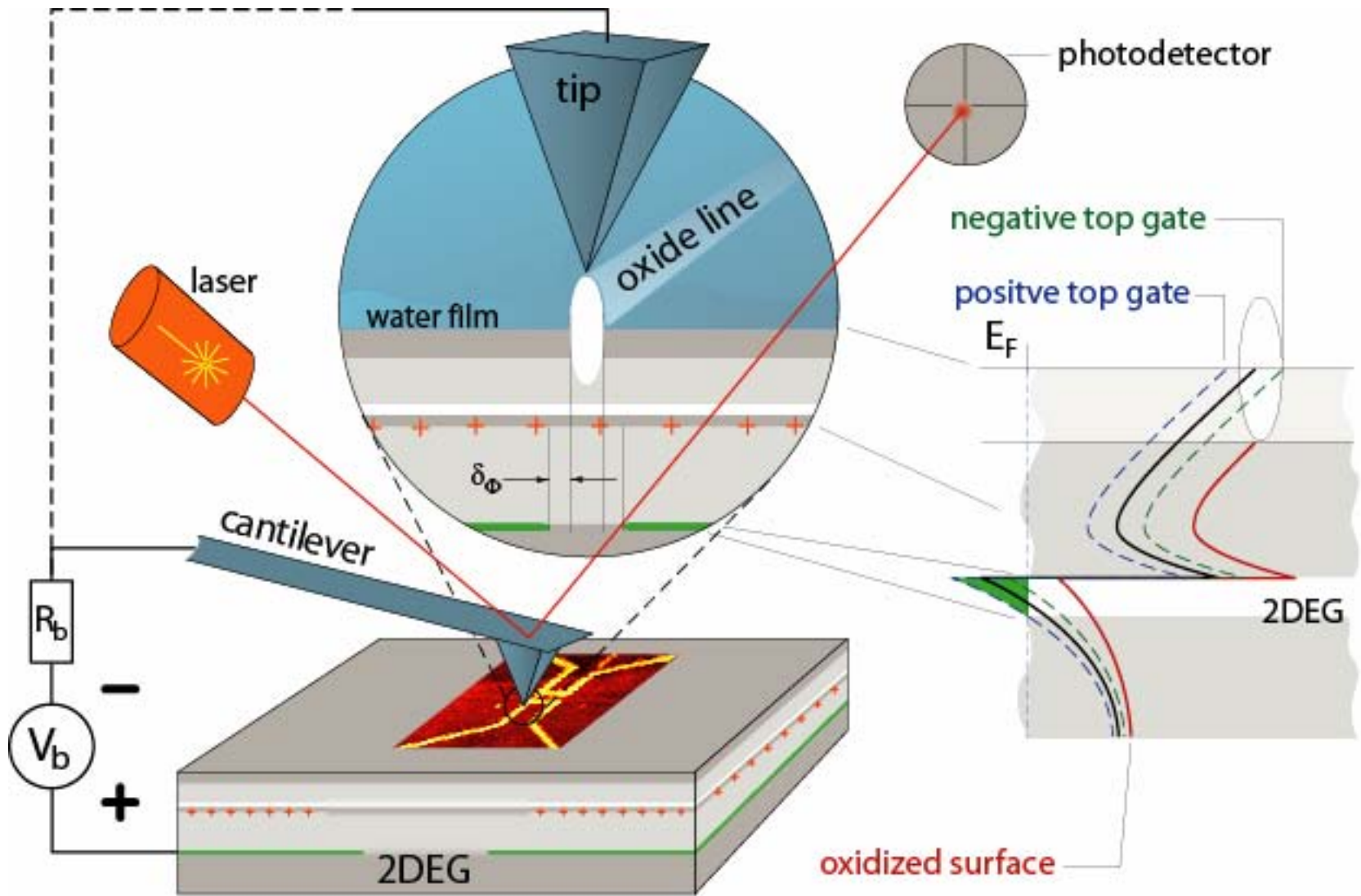


## Requirements:

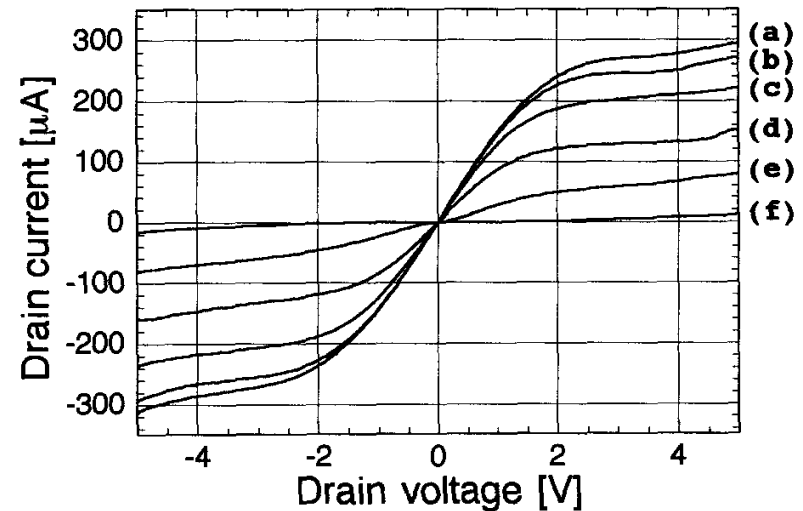
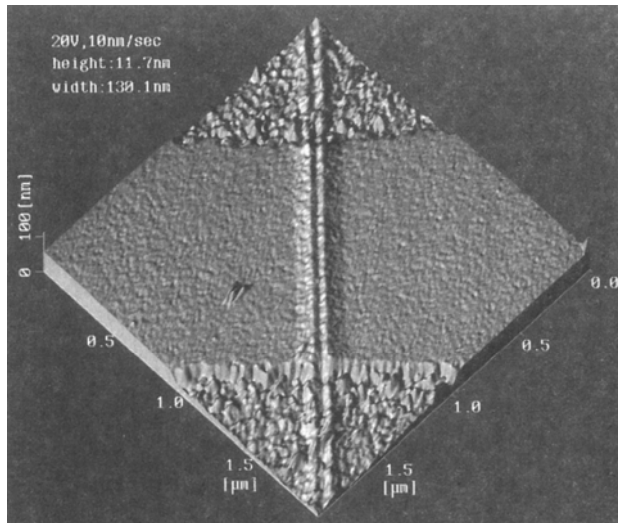
**Controlled humidity 40% - 60%**

**Voltage < -12 V to conductive AFM tip**  
(we use diamond-coated, doped Si tips)





## Local Oxidation of Ga[Al]As:

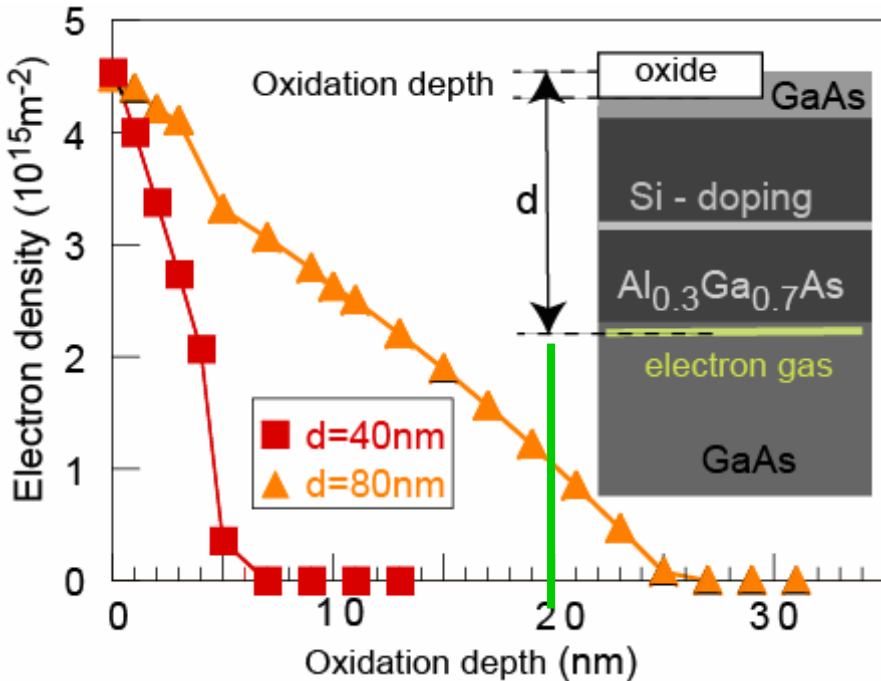


Resistance across line of length  $L$ :  
 $RL \sim 250\text{k}\Omega \times \mu\text{m}$  at 4 K

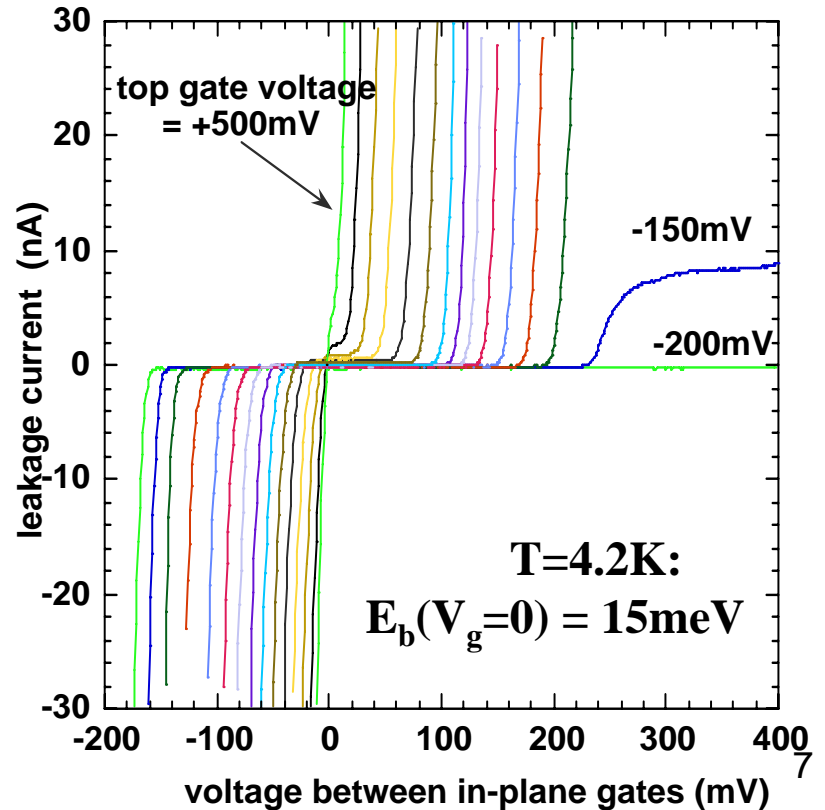
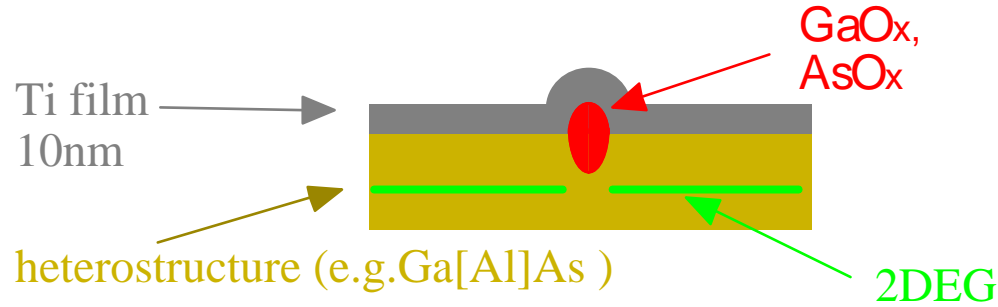
M. Ishii and K. Matsumoto, Jpn. J. Appl. Phys. **34**, 1329 (1995)

# Depletion of the 2DEG in Ga[Al]As:


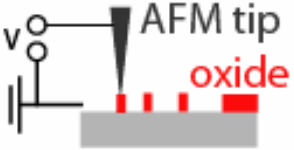









Simulation:



R. Held et al.,  
 Appl. Phys. Lett. **73**, 262 (1998),  
 ibid. **75**, 1134 (1999).



# Some features of lithography by local oxidation :

lithography and etching	lithography and lift-off
1: metallization metal layer, 0,1 	1: resist spin coating <b>AFM lithography</b> 1: oxidation  2: metallization 
2: resist spin coating 	5: lift-off 
3: illumination 	4: etching 
4: development 	5: resist removal 
5: etching 	
6: resist removal 	

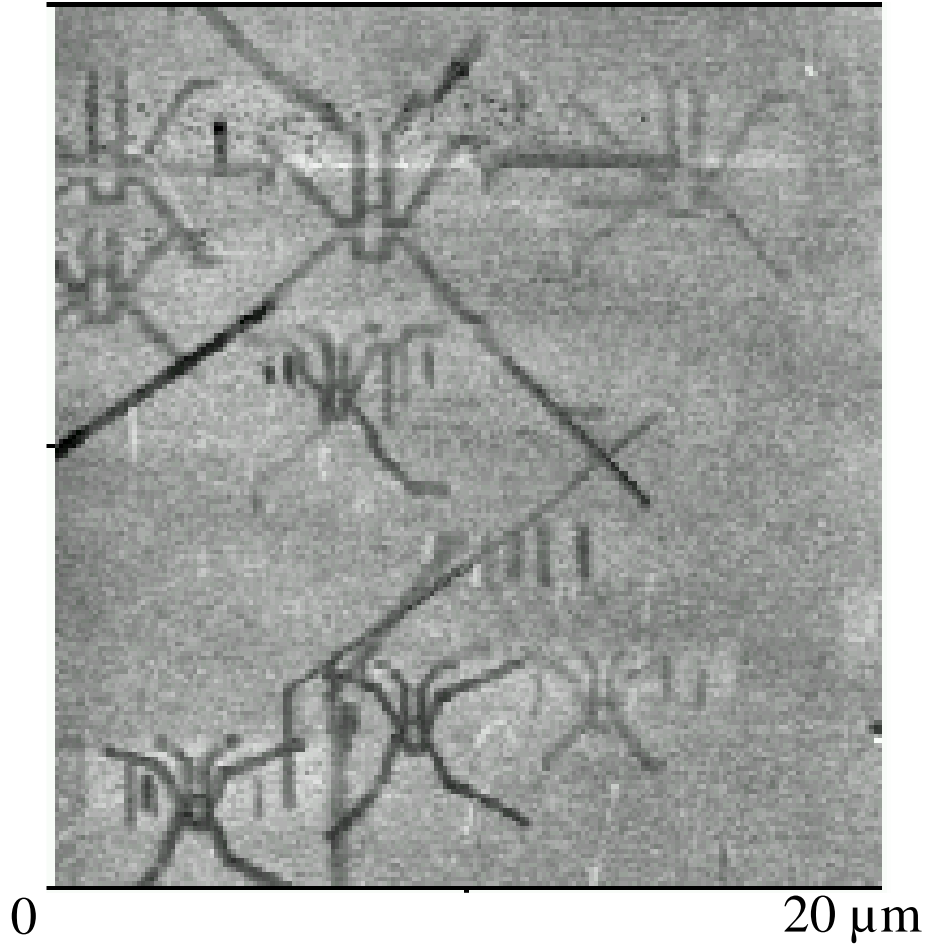
## Advantages:

- no resist
- single step
- simple inspection
- test and change
- in-situ control
- electronic properties...



## On-chip trial and error:

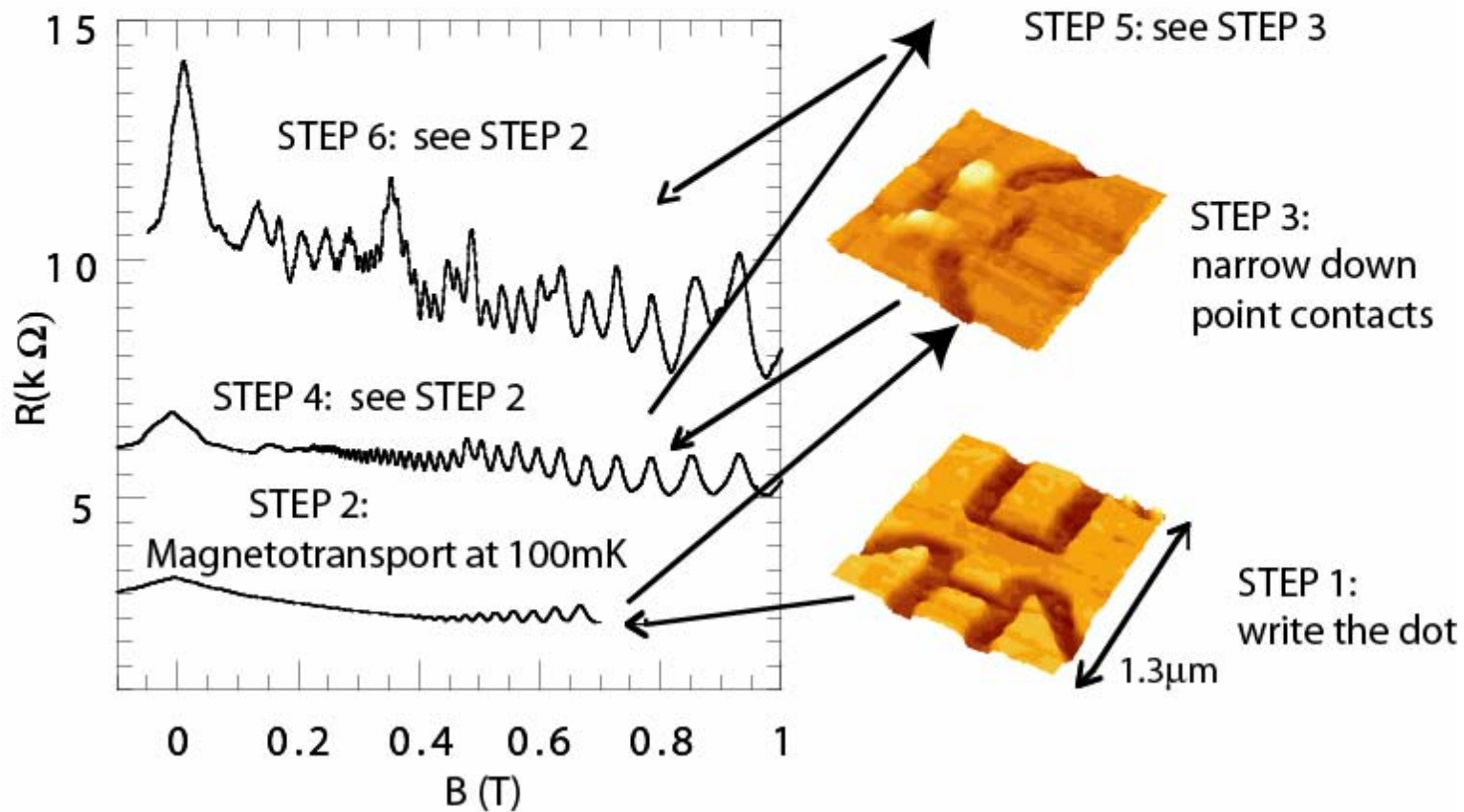
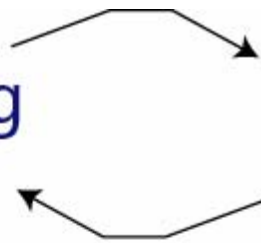
20  $\mu\text{m}$



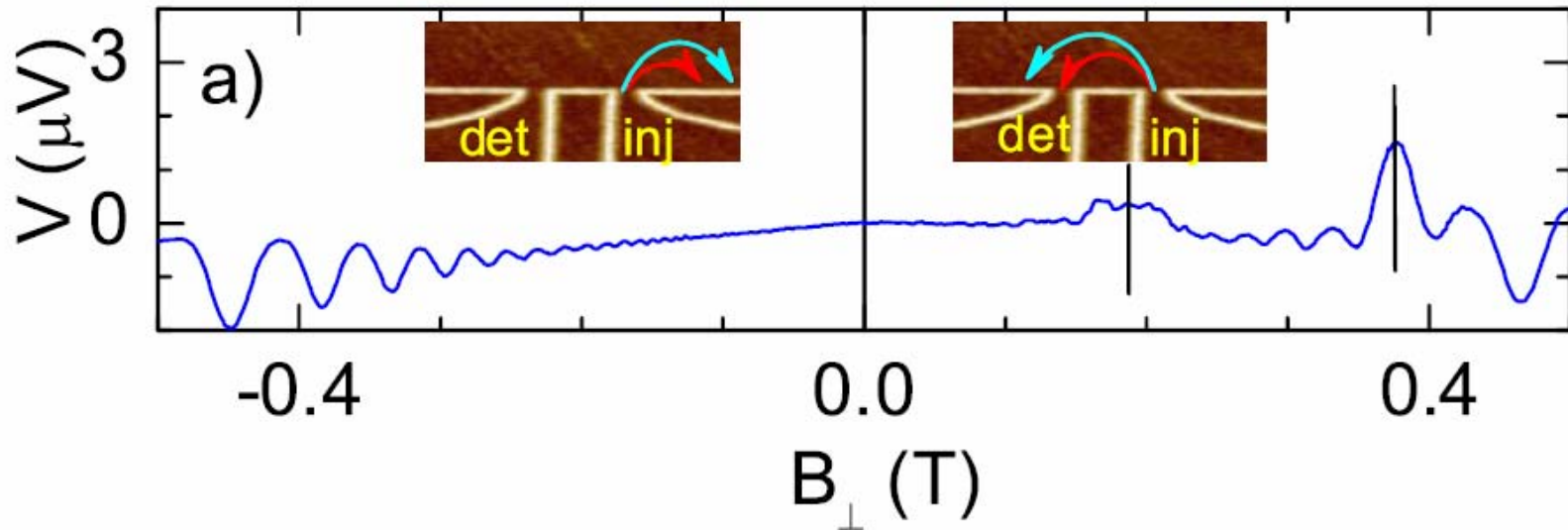
Feedback:

Patterning

Low Temperature  
Measurements

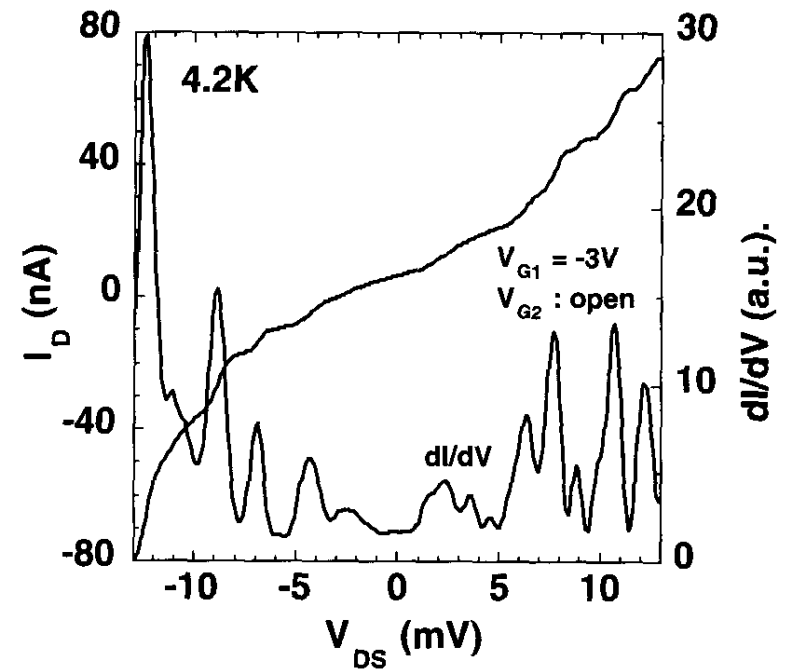
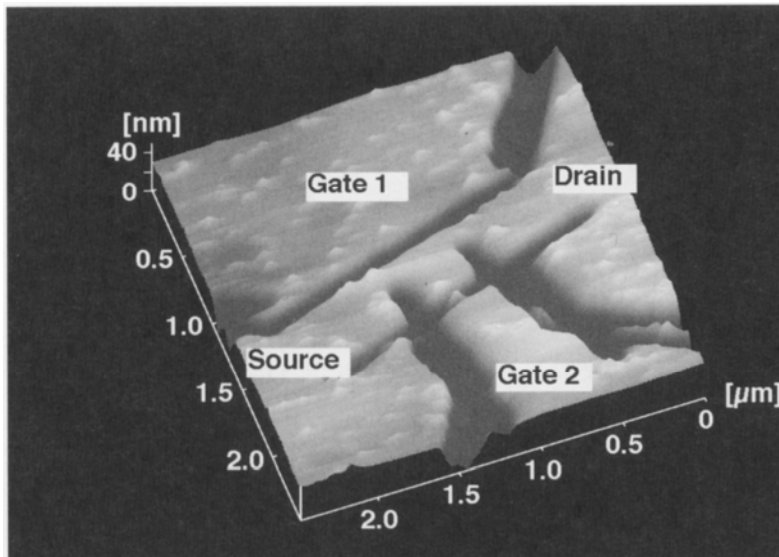


## Ungateable materials: Hole focusing in p-Ga[Al]As



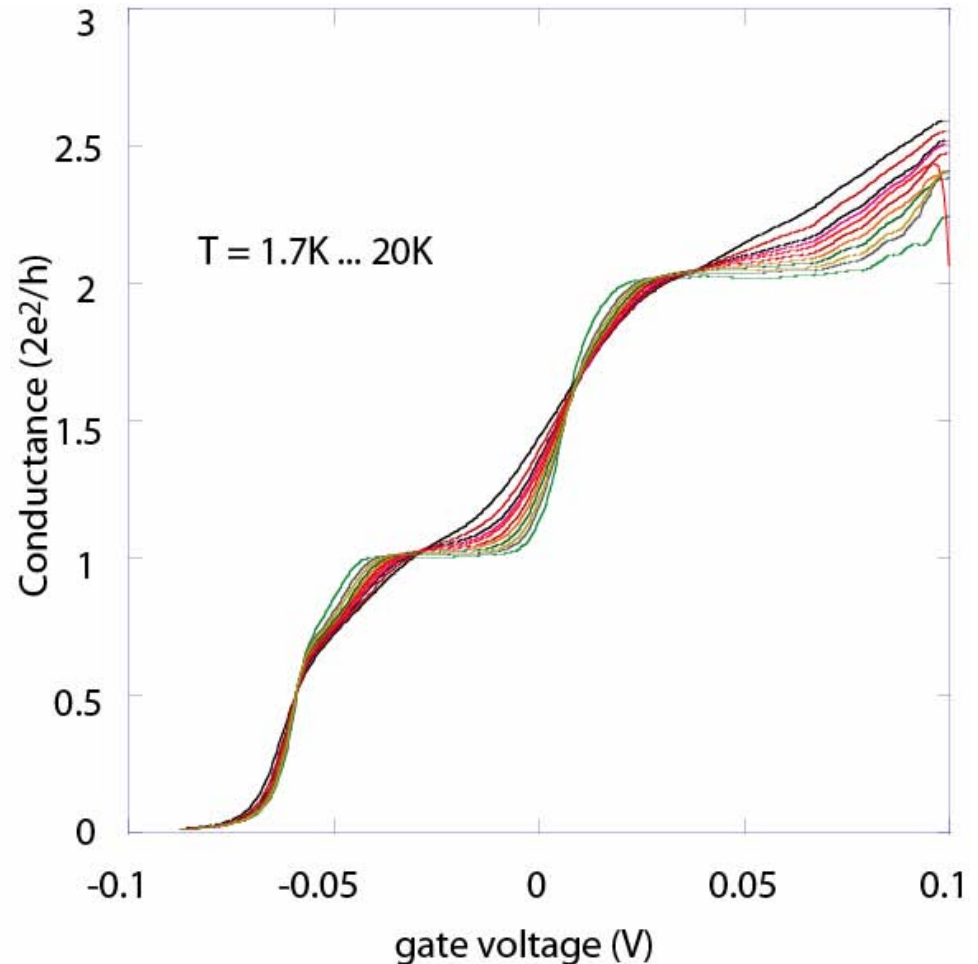
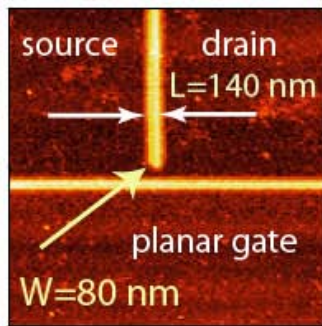
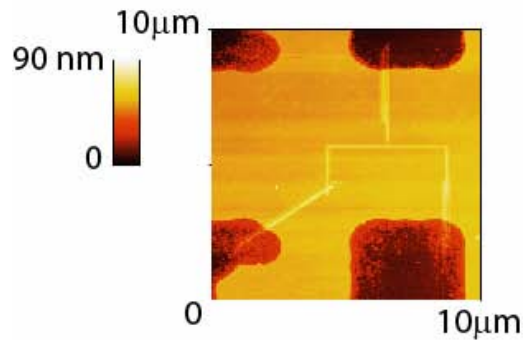
L. Rokhinson et al., Phys. Rev. Lett. **96**, 156602 (2006)

# Other heterostructure systems: Coulomb blockade in an InAs/AlGaSb quantum well structure:



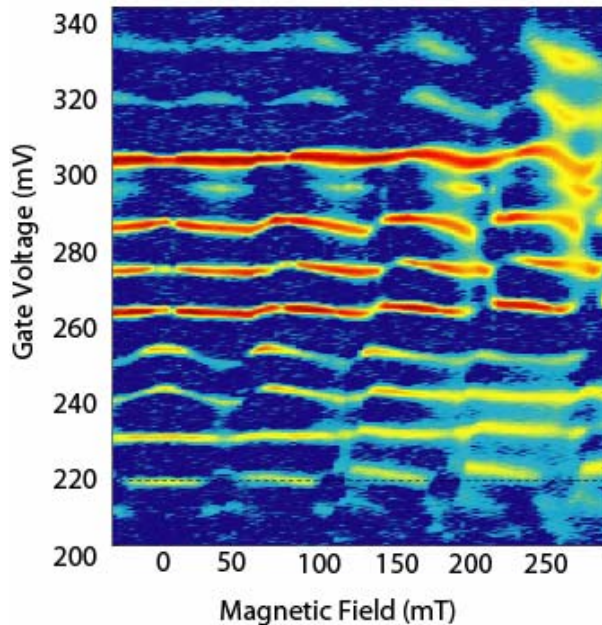
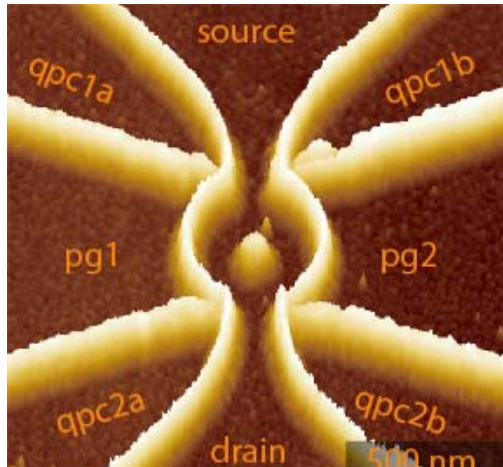
S. Sasa et al., Jpn. J. Appl. Phys. **38**, 480 (1998)

# Electronic properties: For example a quantum point contact:



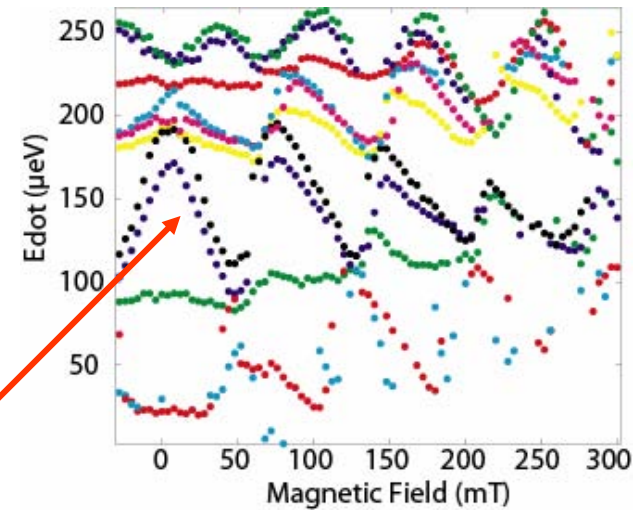
Lateral depletion length  $l_{\text{dep}} = 15 \text{ nm} \ll l_{\text{dep}}$  by FIB or etching  
Steep walls; nonparabolic confinement possible

# Definition of multiply connected nanostructure geometries without etching / air bridges: Coulomb blockade of a quantum ring

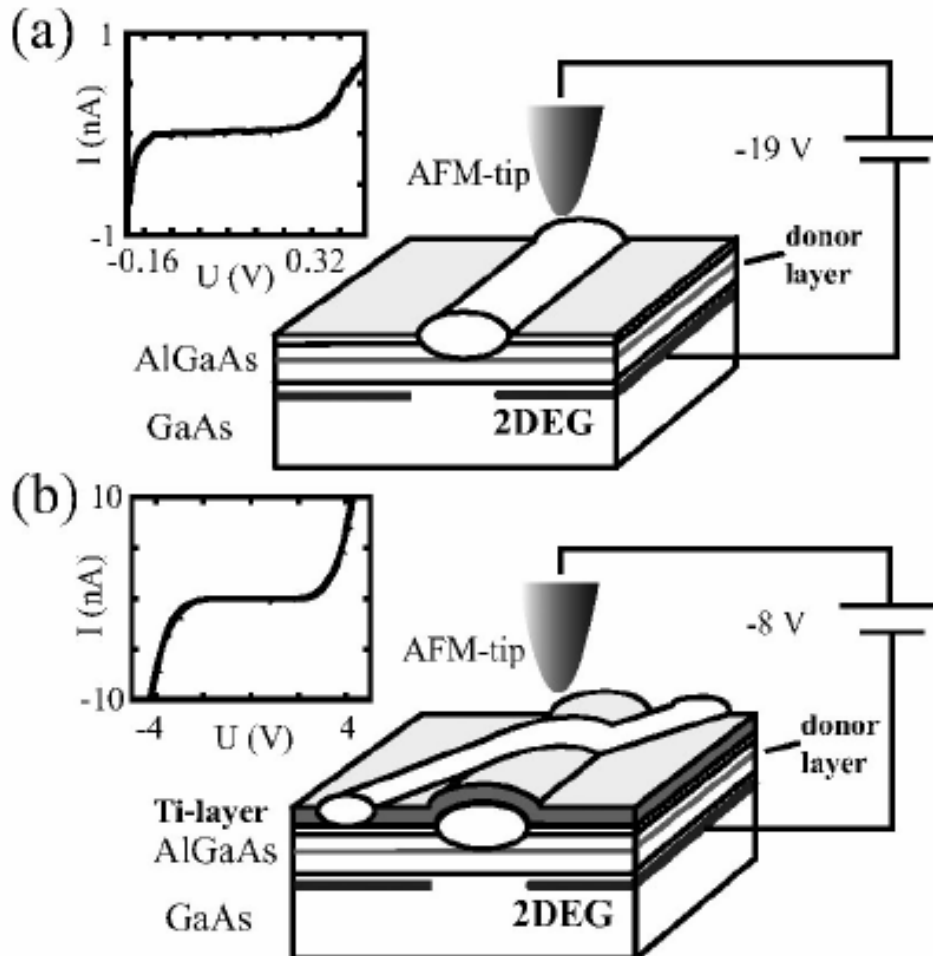


Log(I<sub>sp</sub>/nA)

I<sub>persistent</sub>  
5 nA



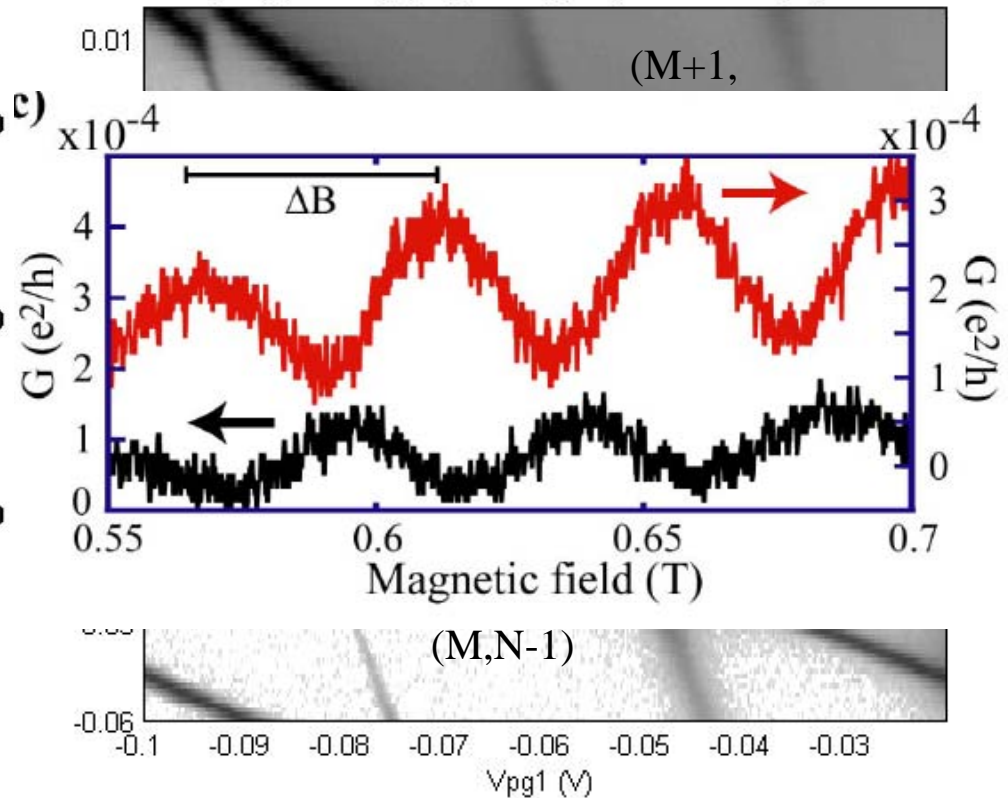
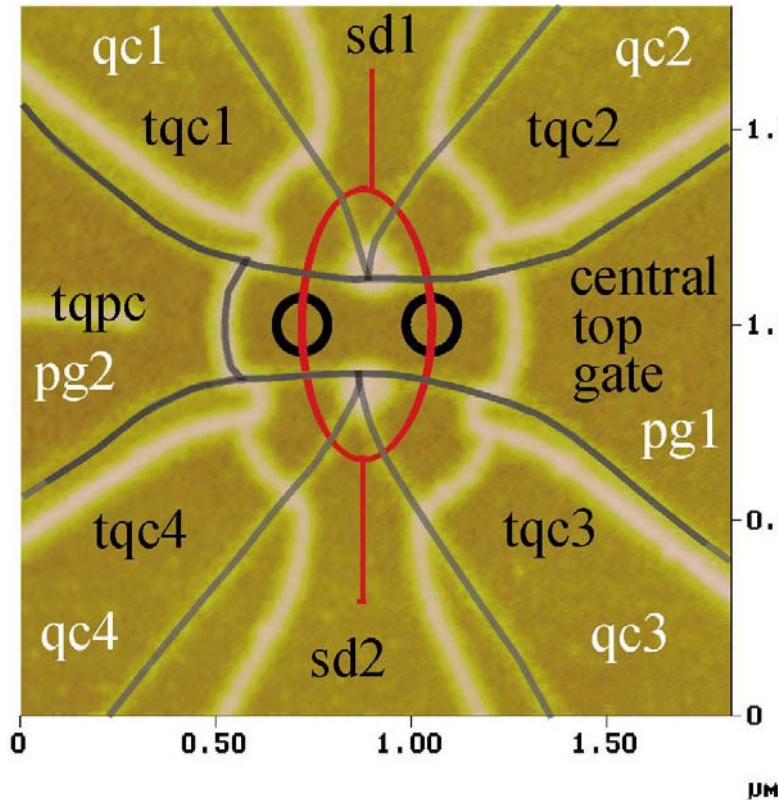
## Double layers of nanostructured electrodes:



1. Local oxidation of the Ga[Al]As
2. Ti film deposition (<10nm)
3. Local oxidation of the Ti layer, aligned.

# Example: coupled quantum dots embedded in a ring: Investigation of coherence in inelastic cotunneling

8 top gates, self aligned, 7 in plane electrodes



Figures: courtesy of T. Ihn, ETH Zurich

Electron number  $\sim 30$

Each dot: Charging energy  $\sim 0.7$  meV  
Single-particle level spacing  $\sim 0.1$  meV



## Summary and Conclusions:

Scanning probe lithography is a powerful complementary technique

### Advantages:

simple: direct writing, single step, see immediately what you get  
in-situ control possible;  
VERY small lateral depletion length, steep walls;  
patterning ungateable samples (InAs, p-GaAs,...);  
simple patterning of multiply connected geometries;  
aligned double layers of nanostructures.

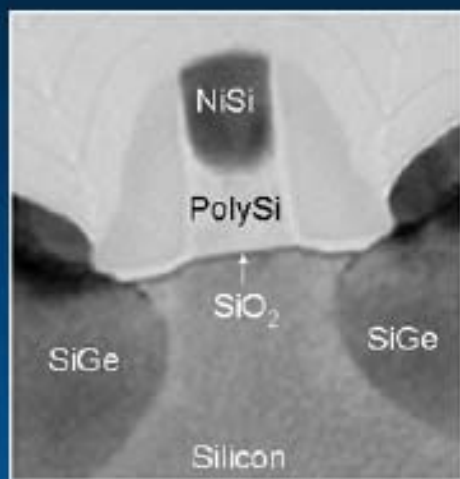
### Disadvantages:

works only for shallow 2D systems;  
serial process, slow;  
(probably) no significant size reduction

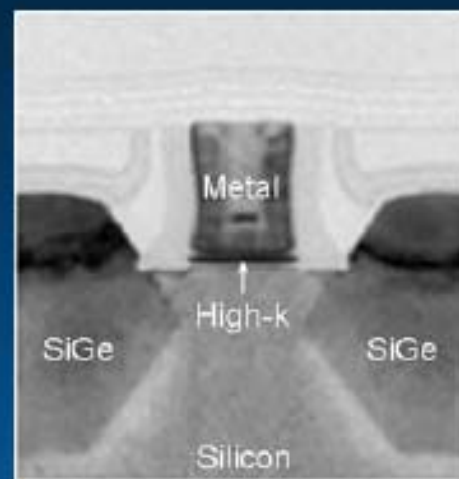
# High-k + Metal Gate Transistors

Improved Transistor Density	~2x
Improved Transistor Switching Speed	>20%
Reduced Transistor Switching Power	~30%

**65 nm Transistor**



**45 nm HK + MG**



Enables New Features, Higher Performance,  
Greater Energy Efficiency

**Own results presented have been obtained in collaboration with:**

Ryan Held

Andreas Fuhrer

Silvia Lüscher

Thomas Ihn

Klaus Ensslin

ETH Zürich

Mihai Cerchez

Stefan Hugger

HHU Düsseldorf

**Thank you for your attention!**