

**JST International Symposium on  
Dependable VLSI Systems 2012**

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**“VLSI design and test for enhanced systems dependability”**

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Program term: FY2007~2014

The “Dependable VLSI Systems” is a collaborative university-industry research program funded by Japan Science and Technology Agency under the CREST\* framework.

- In its 6th year of the 8 year term

\*CREST: <http://www.jst.go.jp/kisoken/crest/en/index.html>

## Attributes, Threats, and Means in Dependability as defined by IFIP:



<b>Attributes</b>	way to assess the dependability of a system
Availability	readiness for correct service
Reliability	continuity of correct service
Safety	absence of catastrophic consequences on the users/environment
Integrity	absence of improper system alteration
Maintainability	ability for a process to undergo modifications and repairs
<b>Threats</b>	things that can affect the dependability of a system
Fault	defect in a system
Error	discrepancy between the intended and actual behavior of a system
Failure	system behavior that is contrary to its specification
<b>Means</b>	ways to increase a system's dependability
Prevention	preventing faults being incorporated into a system
Removal	fault removal during development and removal during use
Forecasting	prediction of faults to remove them or circumvent their effects
Tolerance	putting fault-tolerant mechanisms in place

## Rationale for research in DVLSI

**VLSI:** Is the component key to systems of all kinds. Its dependability is at the foundation of systems dependability.

**Problems:** The dependability of VLSI is actually being increasingly more threatened.

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## **Threats arising from miniaturization**

Variations in dimensions, shapes, doping densities,

Decrease in S/N ratio (radiation, EMI, fixed and floating charges),

Aggravating wear/fatigue phenomena (NBTI, hot carriers, electro-migration).

## **Threats arising from increased complexity**

Enhanced functionality (id, encryption,---)

Multiple- Many-core architecture, multi-thread operation,

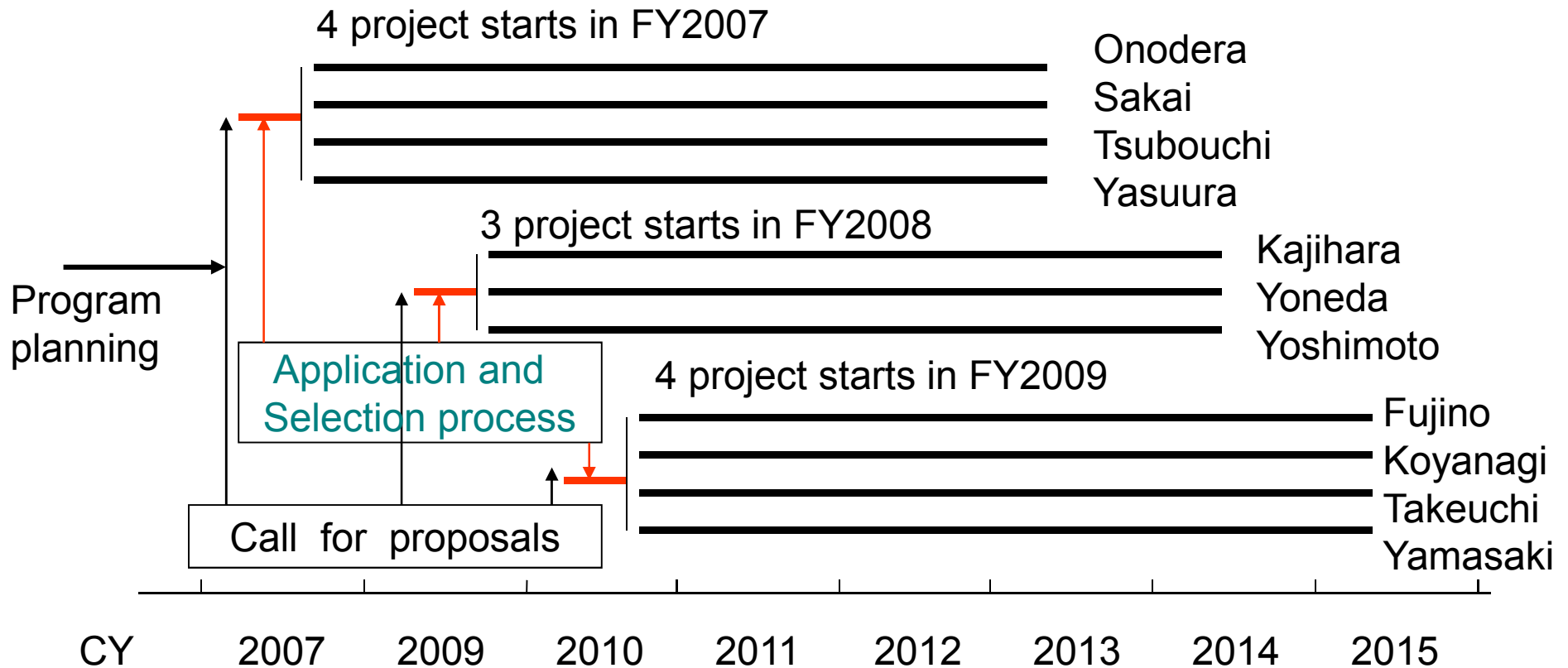
Heterogeneous integration

Analog, digital, nonvolatile, network, sensors, actuators, etc.

Mission of the DVLSI Program:

1. Contain Rising Threats within VLSI (Component Supposed to be Most Dependable) by Design and/or Testing
2. Provide New Functionalities in VLSI which Improve Dependability at the Systems Level

## Selection and Terms of the DVLSI Projects



Program Term: 2007- 2015

**D**VLSI JST/CREST Program 'Dependable VLSI Systems'

# Applications eyed and Approaches taken



Application	Space	Plant Control Transportation	Robot	Auto	Information Telecom	Finance Medical	Consumer
<b>Onodera</b>	Reconfigurable Processor, FF Design, Layout for Manufacturability						
<b>Sakai</b>	Failure-Resistant Architecture, Formal Design Verification						
<b>Tsubouchi</b>		Wide Bandwidth RF, FDE, Coding,, Connectivity, Heterogeneous Interface					
<b>Yasuura</b>	Systems-Level Soft-error Simulation, Soft-error-resistant Circuit/Systems Design						
<b>Kajihara</b>	Design/Test for Field Dependability						
<b>Yoshimoto</b>		Soft-Error-Resistant Memory, Systems-Level Simulation					
<b>Yoneda</b>		Networked Multi-Core Systems					
<b>Koyanagi</b>		Dependable 3D Processor for Image-Recognition					
<b>Takeuchi</b>		Wireless Solid-State Drive, Wireless Interconnect, Wireless Power					
<b>Fujino</b>			Tamper-Resistant Circuits, Tamper-resistance test				
<b>Yamasaki</b>	Real-time OS, controller, and packaging for Hard-Real-Time applications						





Areas DVLSI Projects cover:



Application

System

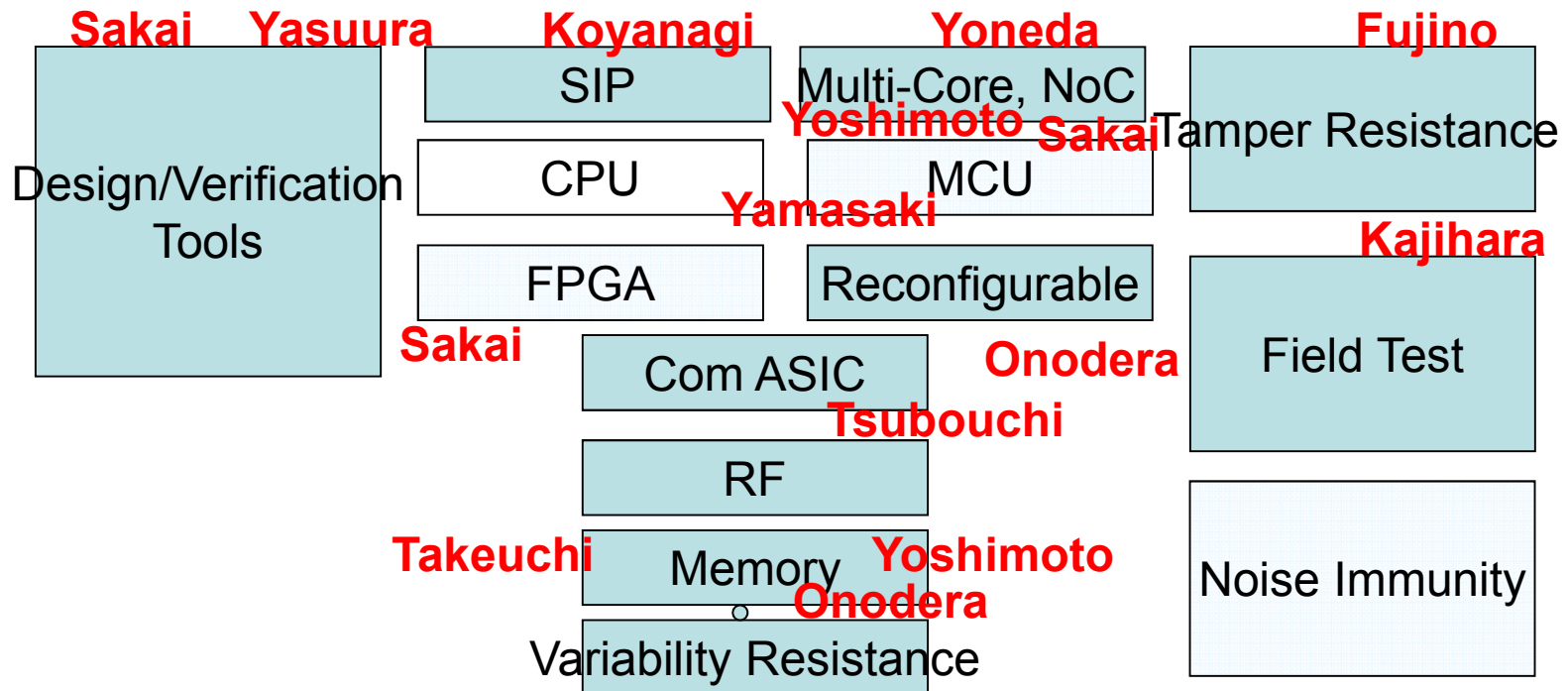
Reconfigurable

Operating System

Real-Time OS

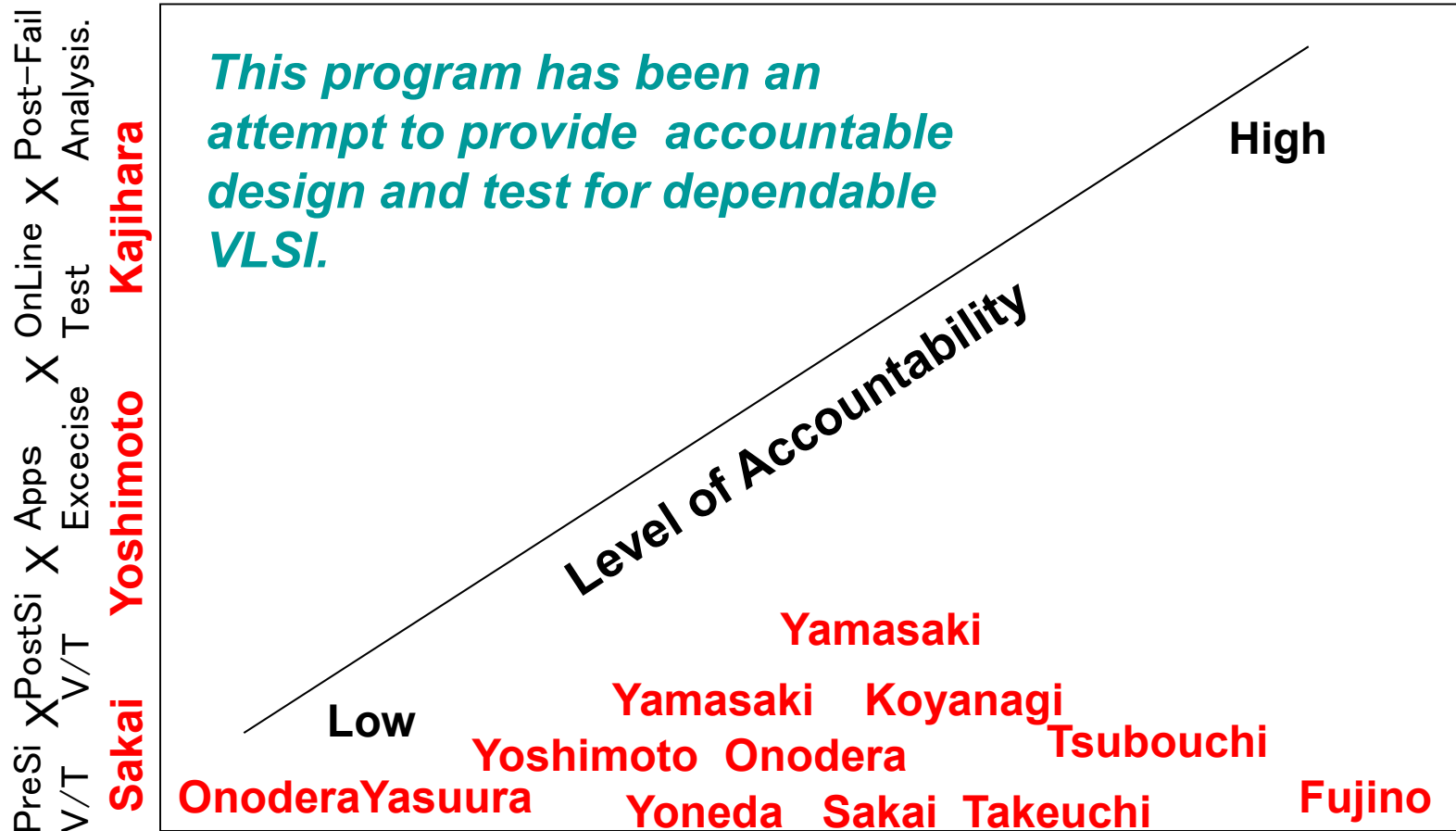
Yamasaki

LSI System



VLSI Dependability =  $\Pi$  (Strength of Means against Threat) x  $\Pi$  (Coverage of Verification and Test)

$\Pi$  Exhaustiveness of Verification, Test



variability soft-error noise redundant connectivity tamper  
 resistance resistance immunity circuits resistance

$\Pi$  Strength of **Means** against Threat (Robustness of Technology)





**Thanks to the Organizing Committee Members:**

**Chair: Hidetoshi Onodera (Kyoto University)**

**Secretary: Masanori Hashimoto (Osaka University)**

**Members: Mitsumasa Koyanagi (Tohoku University)**

**Masahiro Goshima (University of Tokyo)**

**Suguru Kameda (Tohoku University)**

**Hiroshi Oguma (Toyama National College of Technology)**

**Yusuke Matsunaga (Kyushu University)**

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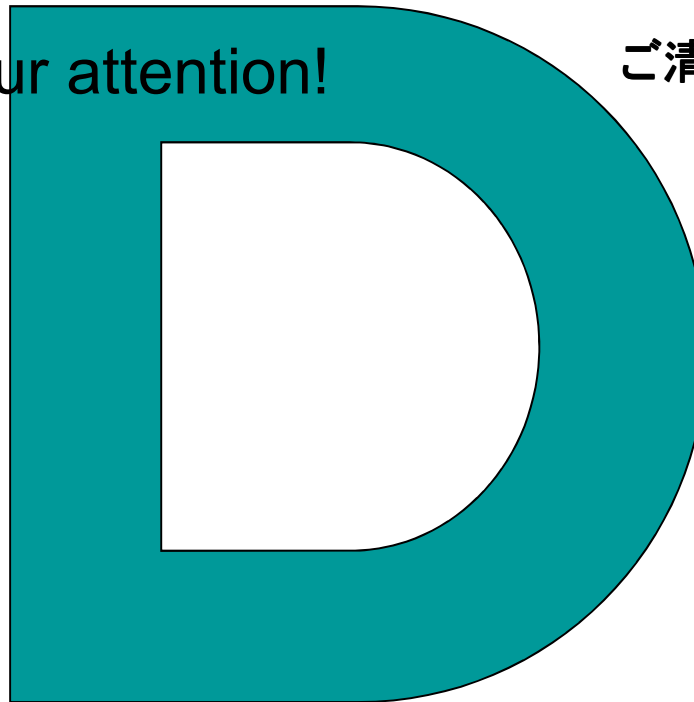


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Thank you for your attention!

ご清聴ありがとうございました



For more details, please visit the URL:

<http://www.dvlsi.jst.go.jp/>

<http://www.dvlsi.jst.go.jp/english/index.html>