Dependable Memory Techniques for Highly Reliable VLSI System

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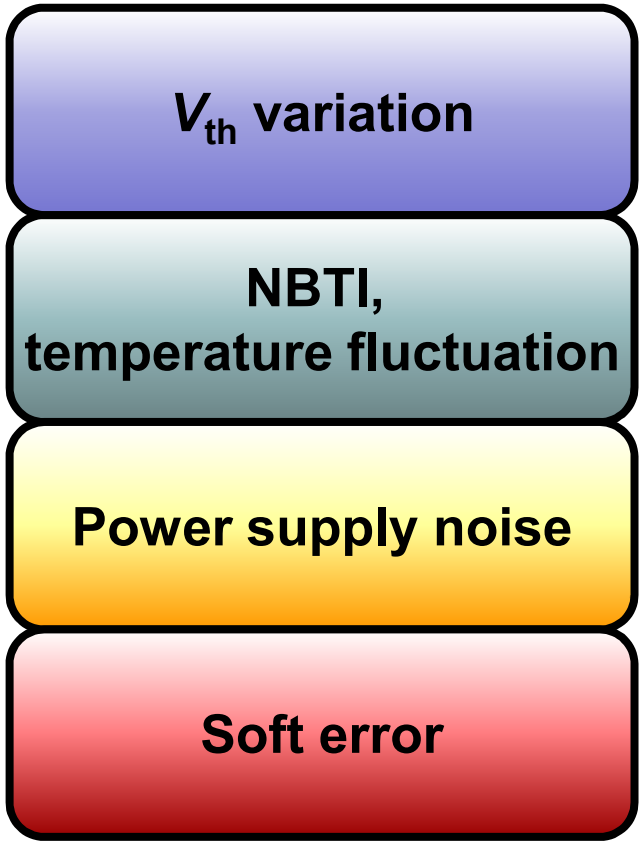
Dependability degradation factor



Improvement / tolerant technique

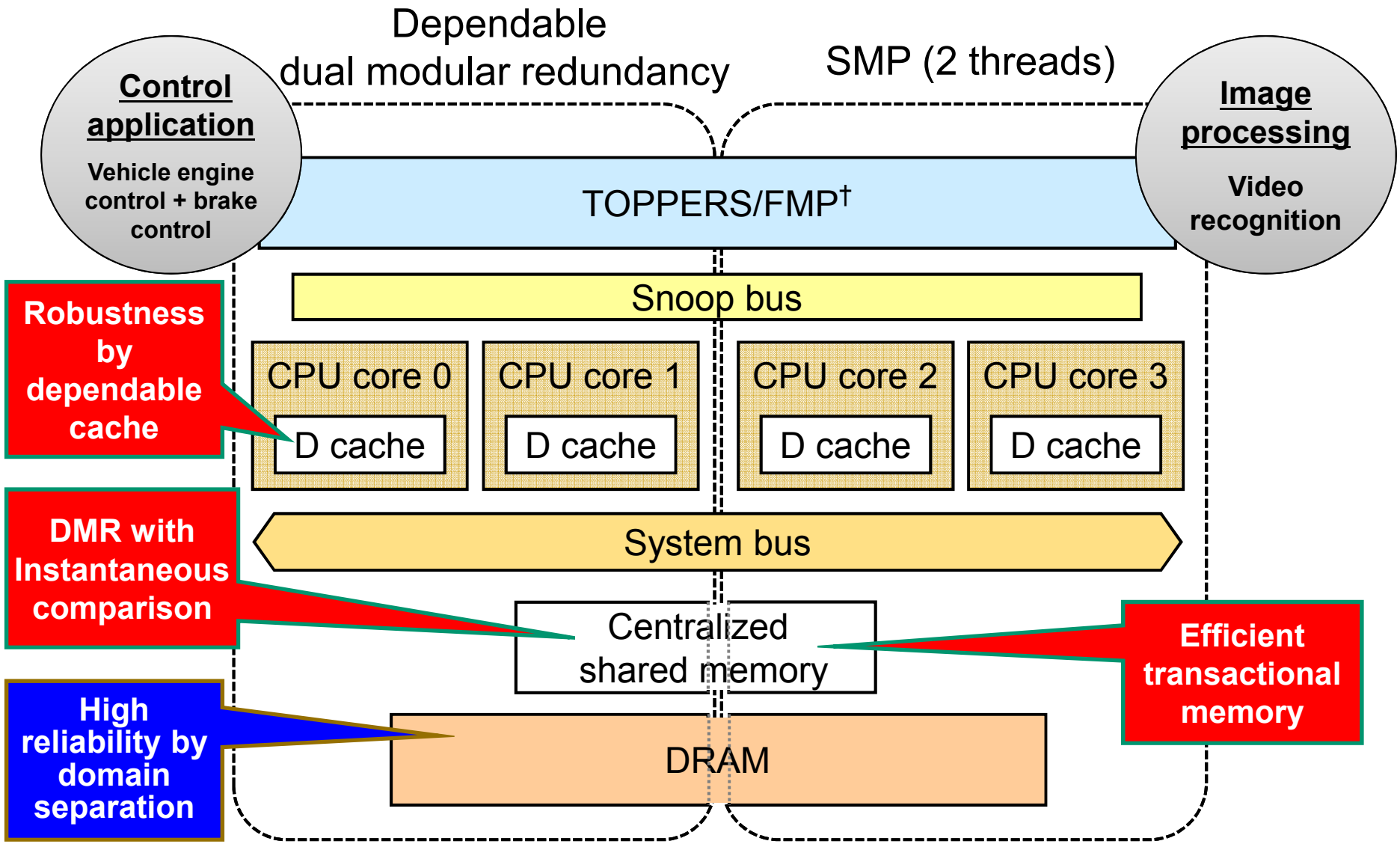
- QoB Cache
- FGVC memory（with BIST）
- Lockstep with QoB multicore

- Power supply noise filter
- Autonomic memory with ODM
- Lockstep with QoB multicore

- Soft error tolerant memory cell
- Lockstep with QoB multicore

QoB: Quality of Bit
FGVC: Fine-Grain Voltage Control

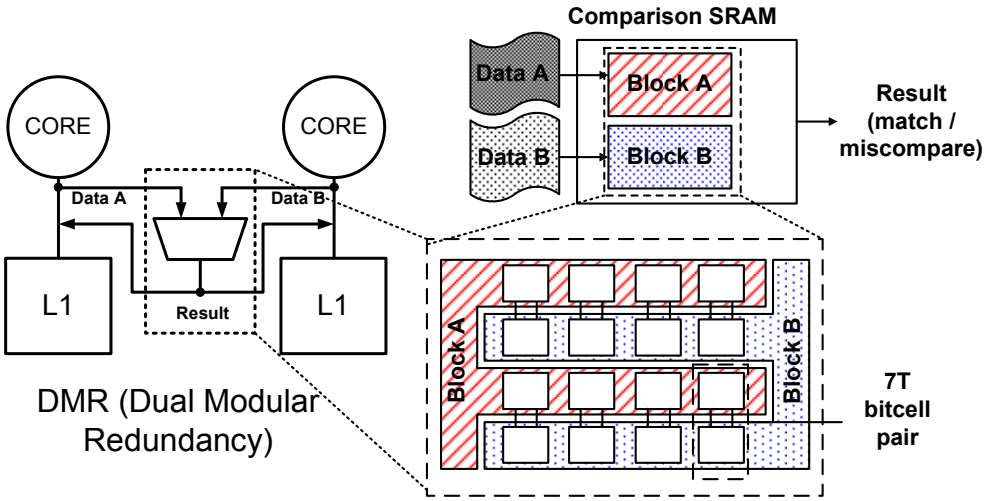
Dependable QoB multicore processor system

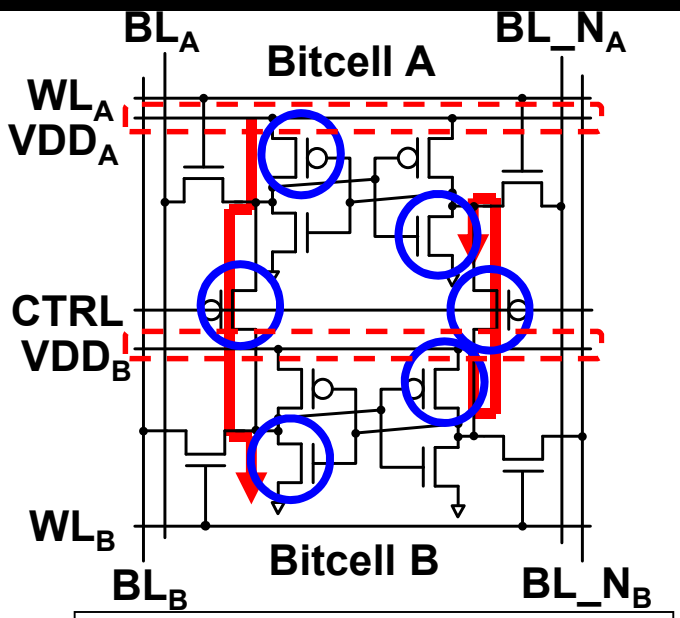


† TOPPERS/FMP: new generation kernels - to provide support for multi-core processors. Both symmetric and asymmetric configurations are supported by TOPPERS project.

Instantaneous Block data comparison (QoB) for Dual Modular Redundancy

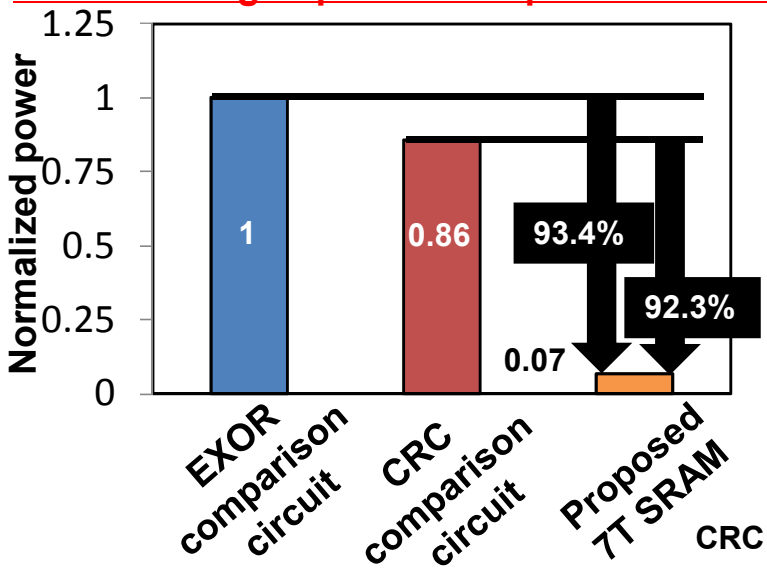
Variation in transistors is a critical issue for a reliability of LSI
⇒DMR is one way to improve the reliability.





When different data are stored, a supply current flows through the connecting pMOSes

Proposed SRAM is useful for DMR,
it realizes high-speed & low-power data comparison.



Detecting miscompare bitcell pair by the supply line voltage

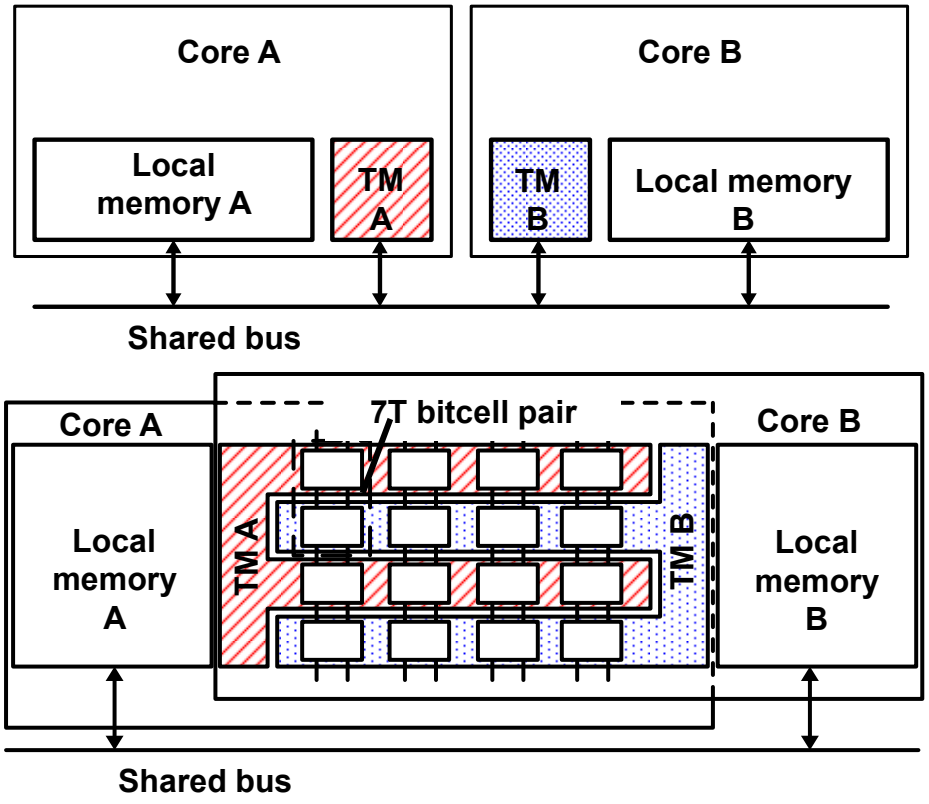
In the proposed SRAM, 8-kb data can be compared in 130ns.

The proposed scheme reduces power consumption by 93.4% and 92.3% compared with EXOR comparison circuit and CRC comparison circuit

CRC : Cyclic Redundancy Check

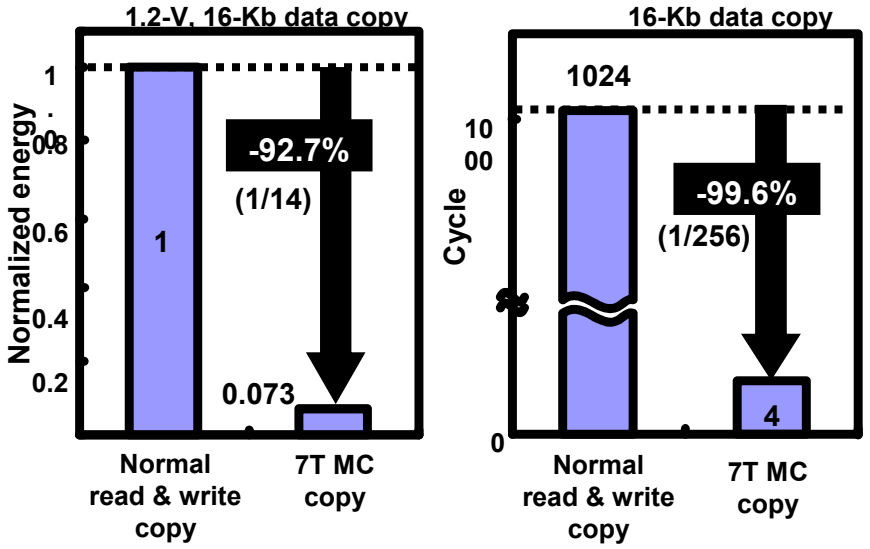
Instantaneous Block data copy (QoB) for Transaction memory

Transaction Memory at multicore processor



(a) general case and (b) copiable 7T SRAM architecture for transactional memory

Apply to instantaneous data copy scheme.

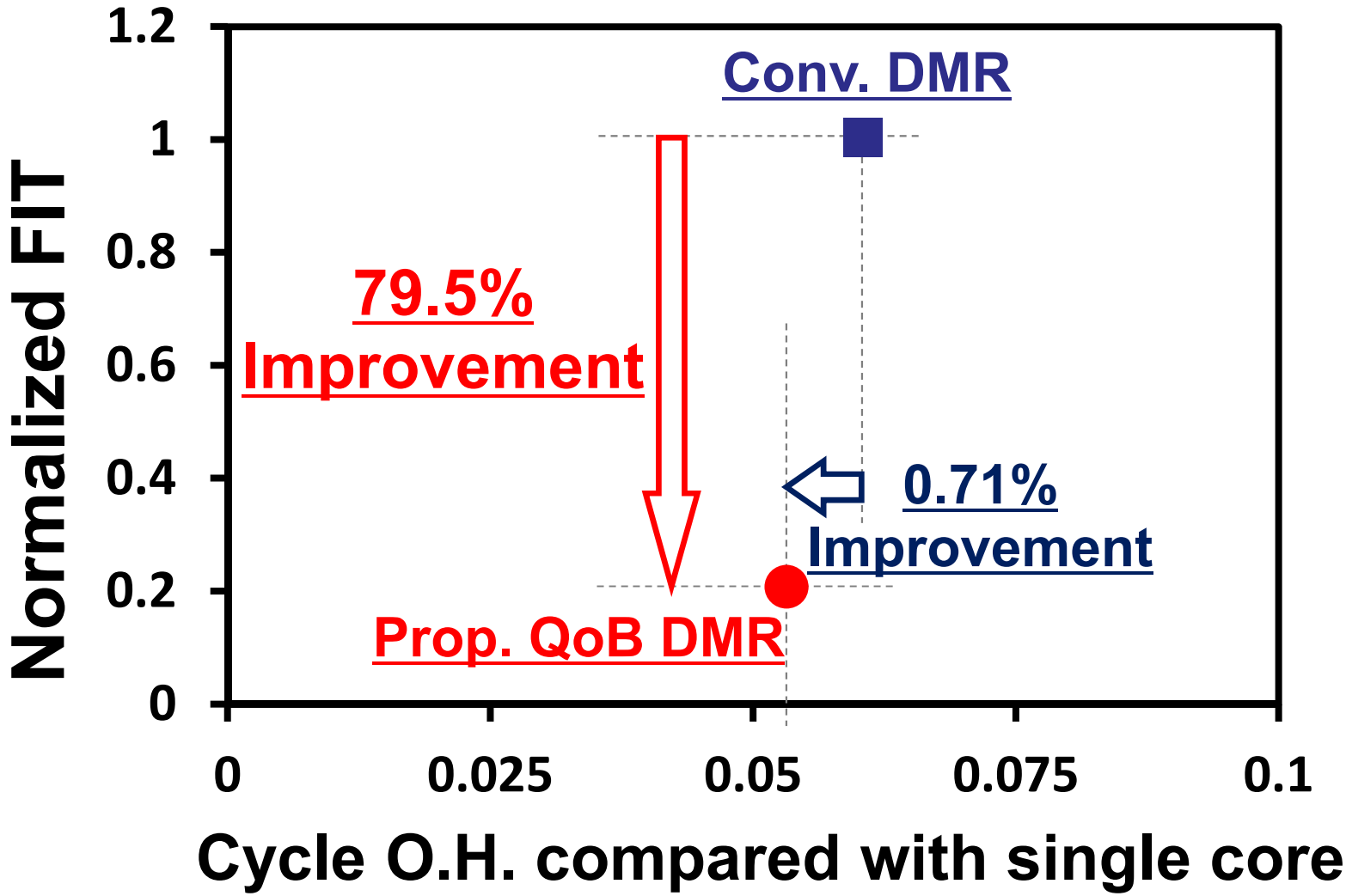


In transaction memory, high speed recovery without shared bus is realized.

Data copy energy is saved 92.7%.
Copy cycle is saved by 99.6%.

FIT and cycle O.H. improvement of QoB DMR

At higher SRAM FIT (low op. voltage) situation



FIT and cycle O.H. improvement of QoB DMR

At lower SRAM FIT (nominal op. voltage) situation