JST CREST/DVLSI

Architecture and Circuits for Dependable 3D-VLSI

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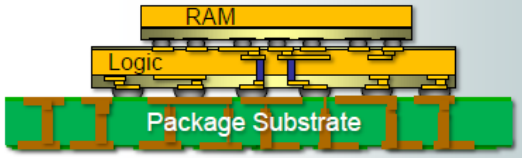
Why 3D ?

What Does 3D Buy Us?

- Connectivity
- Capacity
- Crossovers



Is the Future Repartitioning ?

Byran Black, CTO of AMD at Global Interposer Conf Nov 2011

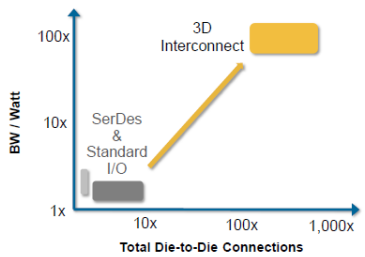
Black claims that AMD has been involved in 3D for more than 5 years but adds that they are "... intentionally not talking about what we're doing."

"Southbridge (22 nm) is probably the last chip that will be impacted by scaling"

In the future focus will be on specific application functionalities to: - -
- reduce mask layers
- reduce run time, power requirements, area and cost
- increase yield while improving performance

These separately fabricated functionalities will be combined vertically and/or horizontally on an interposer to form the final circuit function.

Connectivity: Enables High Bandwidth, Low Power Die-to-Die Communication

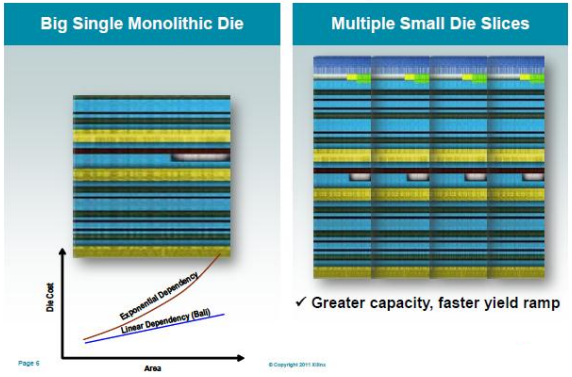


100x bandwidth/watt advantage over conventional methods

Capacity Beyond Moore's Law

Big Single Monolithic Die

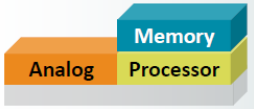
Multiple Small Die Slices



✓ Greater capacity, faster yield ramp

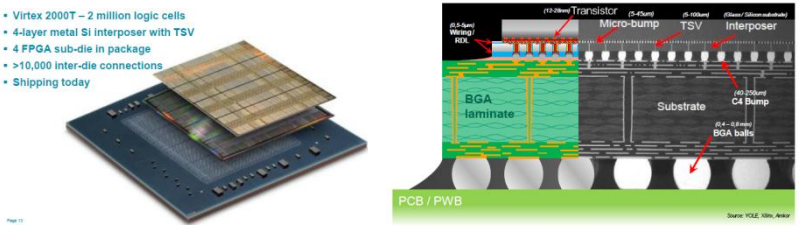
"Crossover SoCs" with Heterogeneous Die

✓Mixed functions

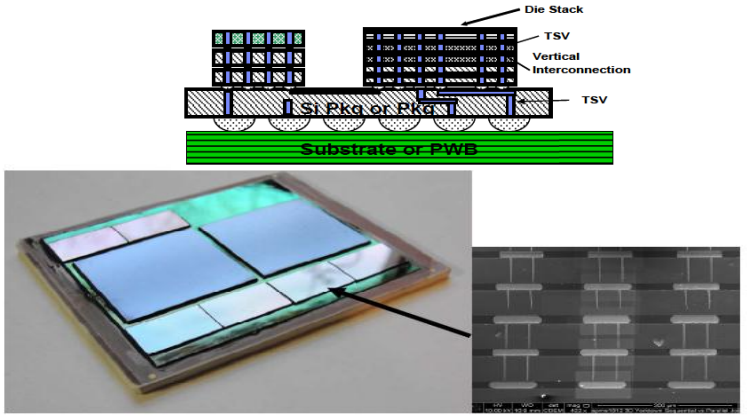


✓Mixed processes

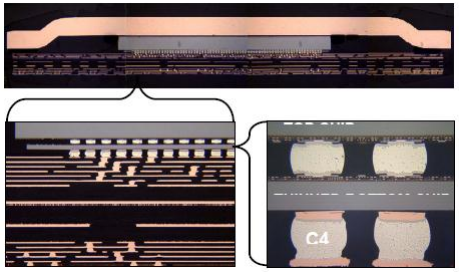
Ivo Bolsens (Xilinx CTO), 3D-Architectures for Semiconductor Integration and Packaging, San Francisco, December 12-14, 2011

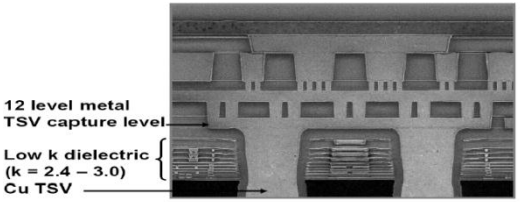


2.5D and 3D FPGA (Xilinx)

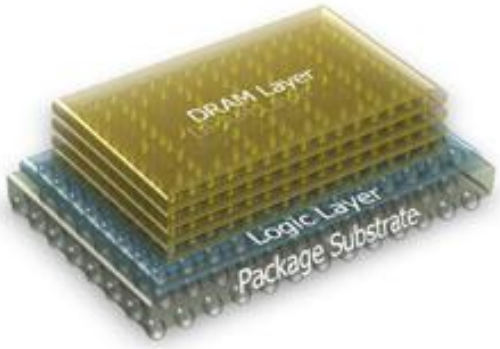


3D System Integration (IBM)

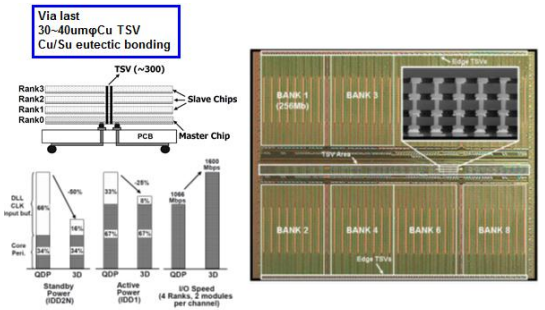




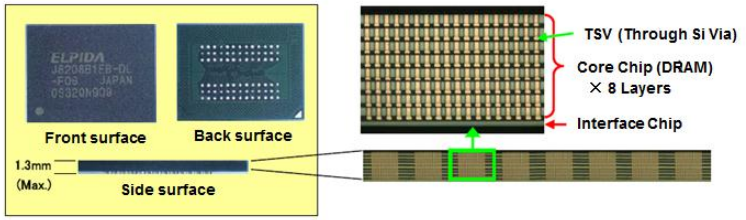
3D-eDRAM for L3 Cache (IBM)



Hybrid Memory Cube (HMC) (Micron+Samsung+IBM)



3D DRAM (Samsung)



3D DRAM (Elpida)

Dependability Related Concerns in 3D VLSI

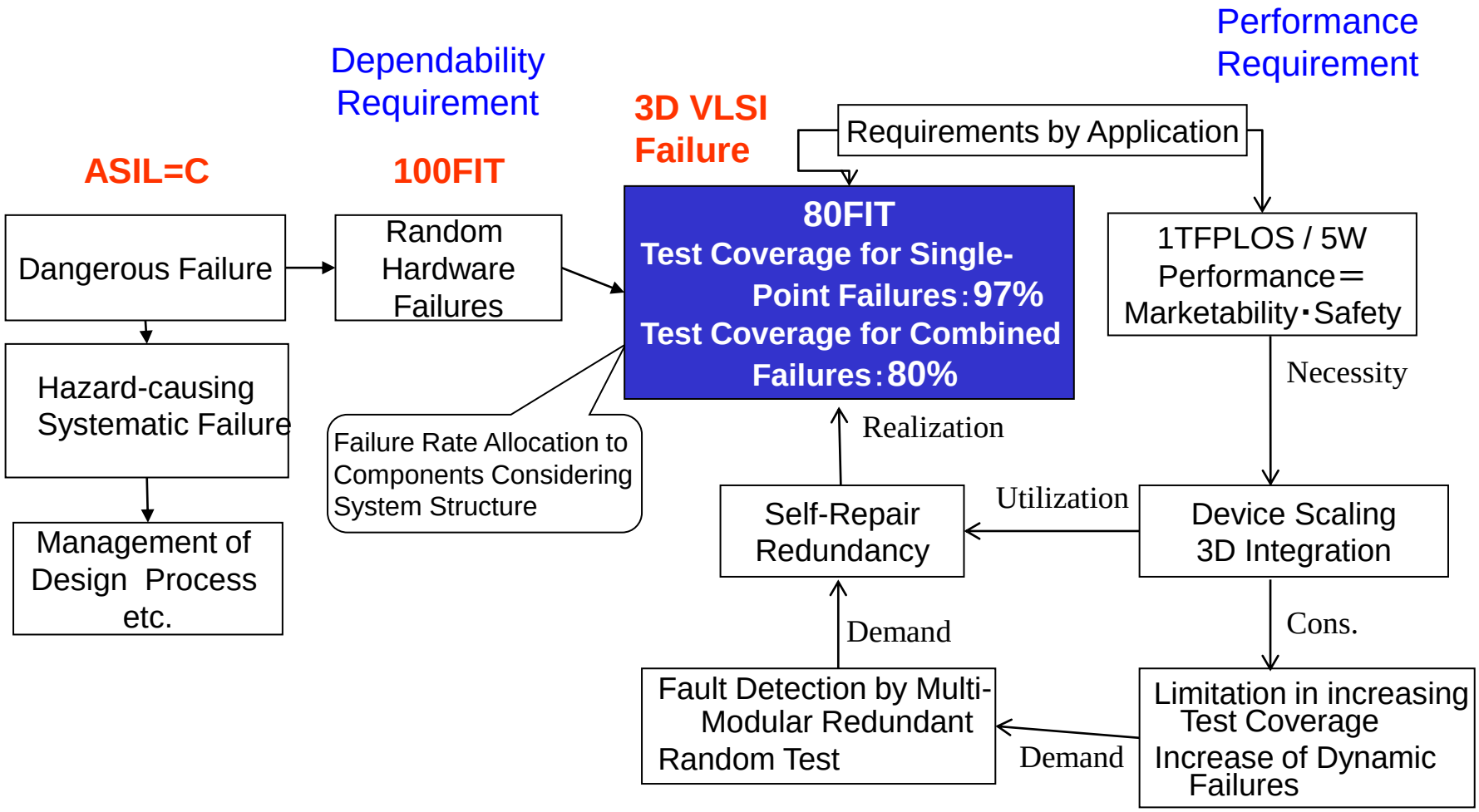
- Heat accumulation and heat removal
- Influences of mechanical stress
- Metal impurity contamination
- Reliabilities of TSV's and metal microbumps
- Design methodology and design tools
- Testing and test design

Dependability is Key Issue in 3D VLSI !

Architecture and Circuits for Dependable 3D-VLSI

Application of 3D VLSI to Image Processing VLSI for Automobile

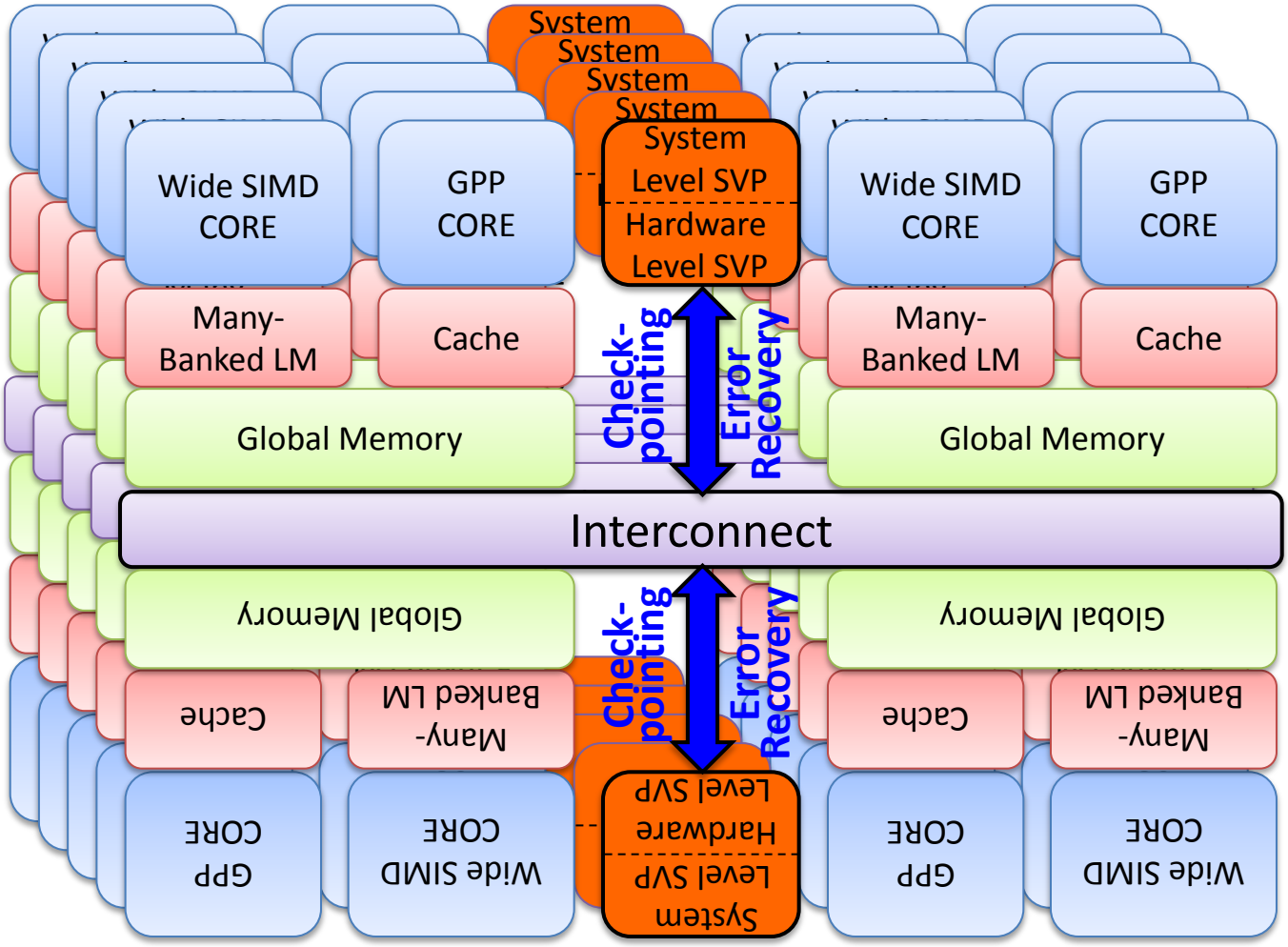
Target : ISO 26262 ASIL=C



<Relation between Requirements by Application and Various Technologies>

After T. Kamada (Denso)

Architecture of 3D DVLSI System



After Prof. H. Kobayashi (Tohoku Univ.)

The Measure for A Reliability Target

・Fault converge 97%

The classification of the error factor

Dynamic failure	Soft error
	Hot spot
	Migration
Static failure	Inspection vector lack
	Insufficient in a verification condition

It corresponds by the multiplexing majority.
- Throughput in 16mS
- Reliability of a majority circuit

It is assisted by run time execution.

The classification of the inspection technique

Multi-plexing	JTAG	TSV
	LBIST	Logic
Majority	MBIST	Memory
Majority	(New)	SVP

The dynamic error case in a car
-Since a power supply variation goes into the place where connection deteriorated ,then a circuit malfunctions.
- A timing error occurs in a hot spot.

The control cycle of a display system is usually 16mS.
If an operation support system also applies to this,
Then it recovers within 16mS is no problem.

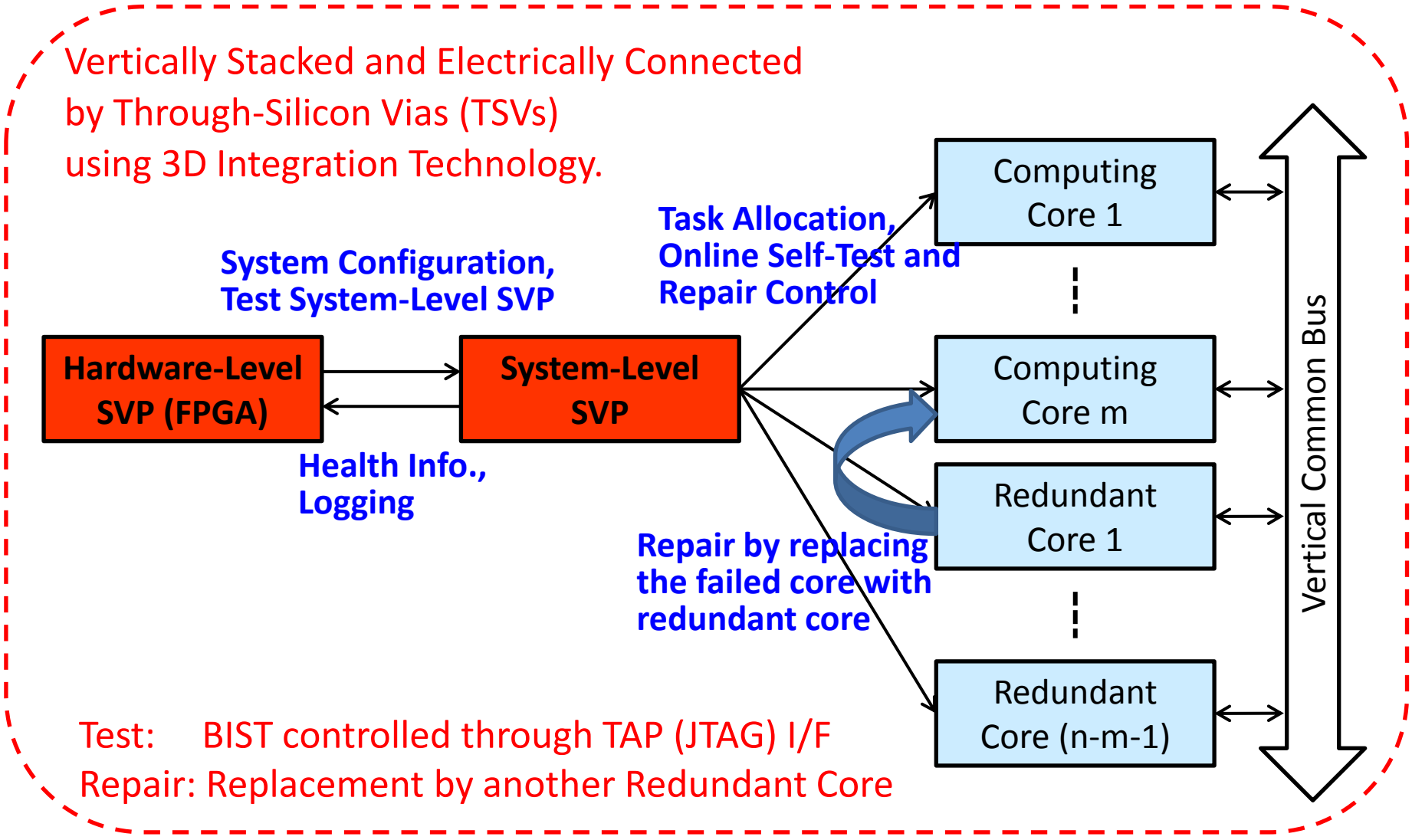
・**80FIT**

The case where failure is overlooked.	The double failure which induces the same result occurs.
	A majority circuit breaks down to the danger side.
The case which failure cannot relieve.	insufficient throughput
	insufficient spare circuit

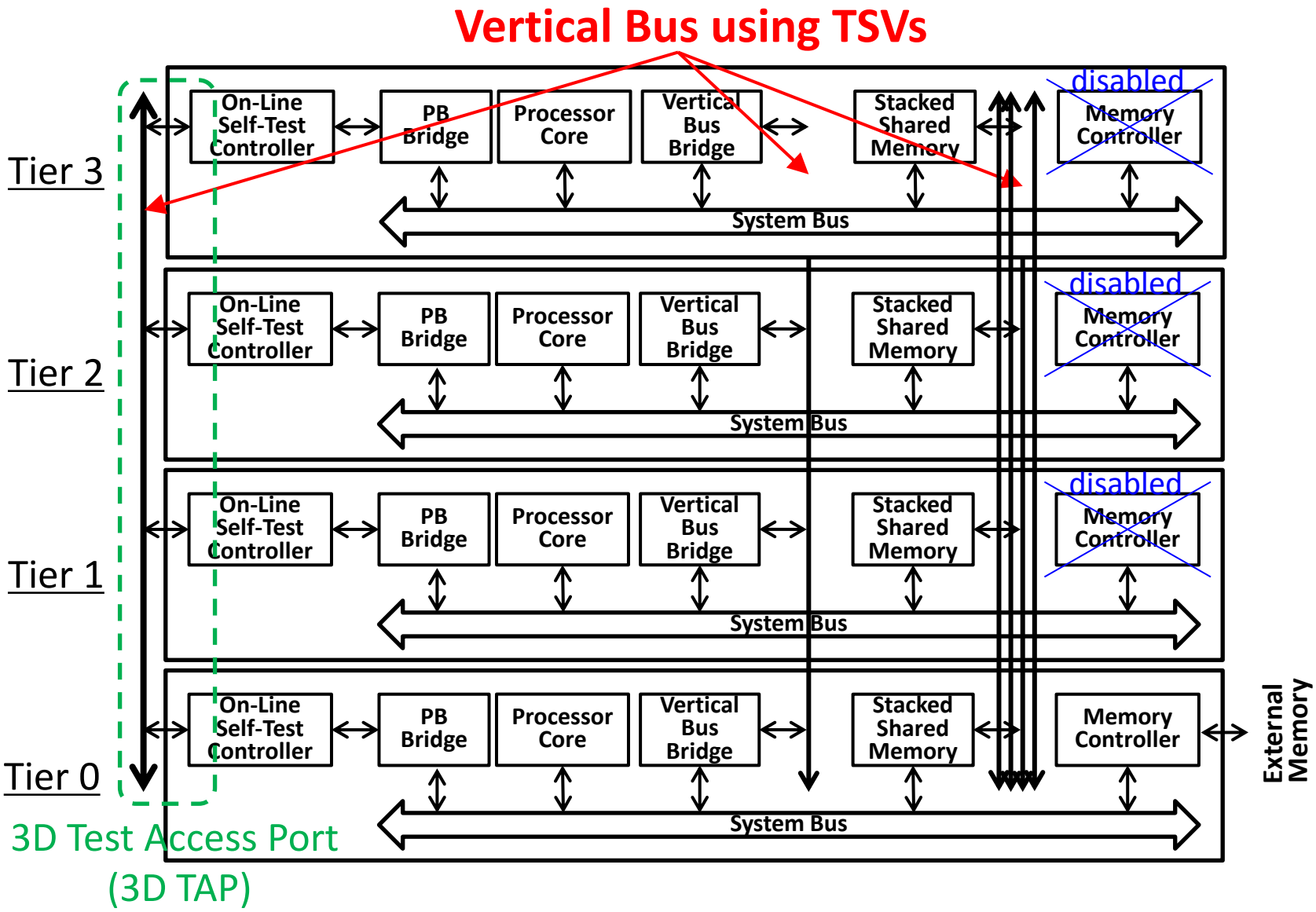
Quantitive analysis is needed.
↓
It comes back to the reliability of a majority circuit, and throughput/parallelism.

After T. Kamada (Denso)

Test Architecture for 3D VLSI with Redundant Tiers



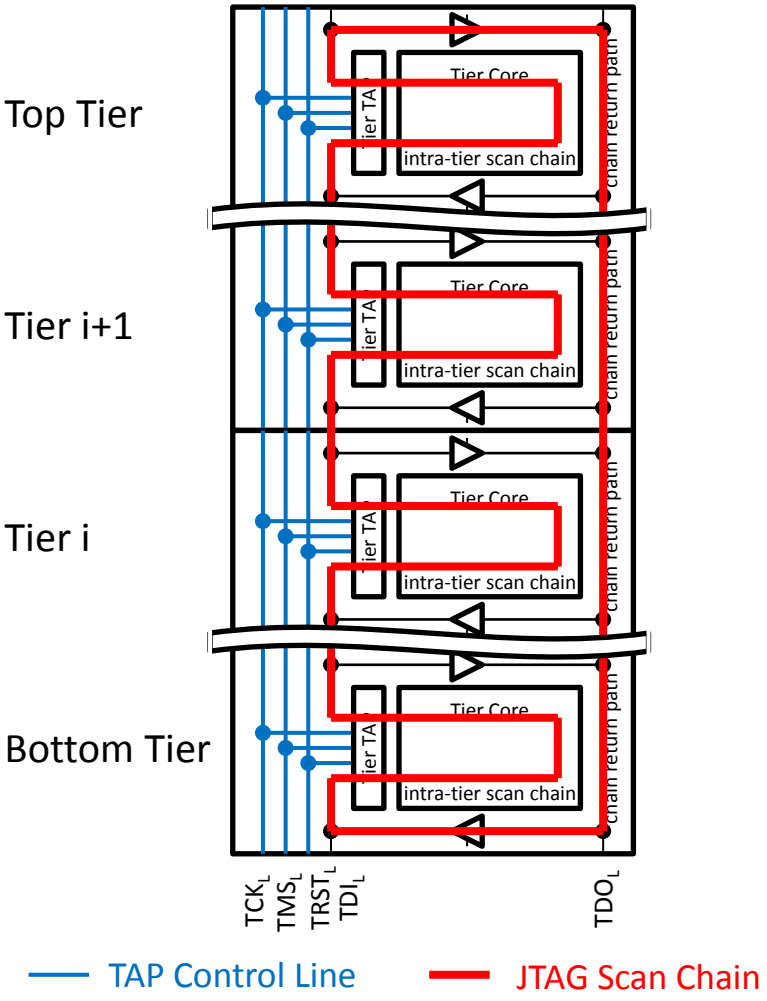
Block Diagram of 3D DVLSI (e.g. 4tiers)



Self-Test Control by System-Level SVP in 3D Dependable VLSI System

- SVP (Supervisor Processor) controls TAP and Chain in the stacked 3D dependable LSI
  - Drives TCK, TMS, TRST, TDI
  - Read TDO to get test data registers in the stacked dice

✓ Assuming TAP signals are connected by quadruple TSV that has much higher reliability than single TSV



3D DfT Architecture

Functional Design

- ≥4 Stacked Dies, Core-Based
- Inter-Connect: TSVs
- Extra-Connect: Pins

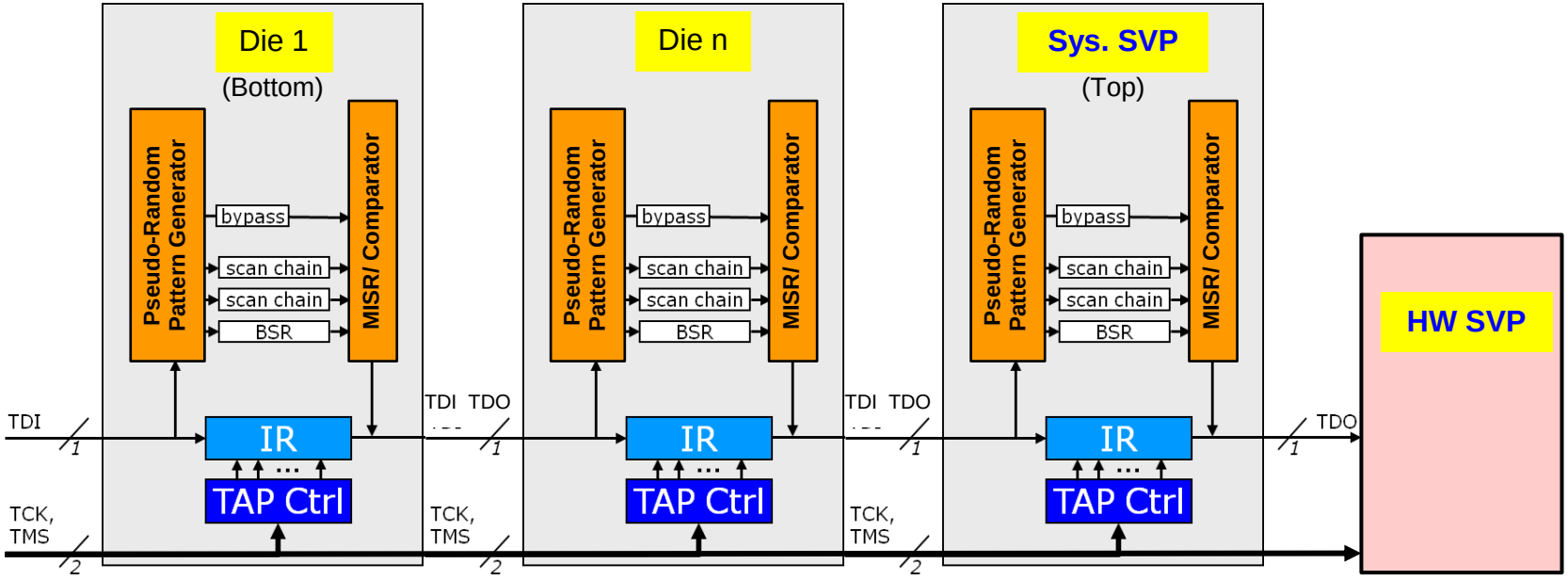
Existing Design-for-Test

- Core: Internal Scan, TDC, LBIST, MBIST;
  IEEE 1149.1 wrappers, TAPC
- Stack Product: IEEE Std 1149.1

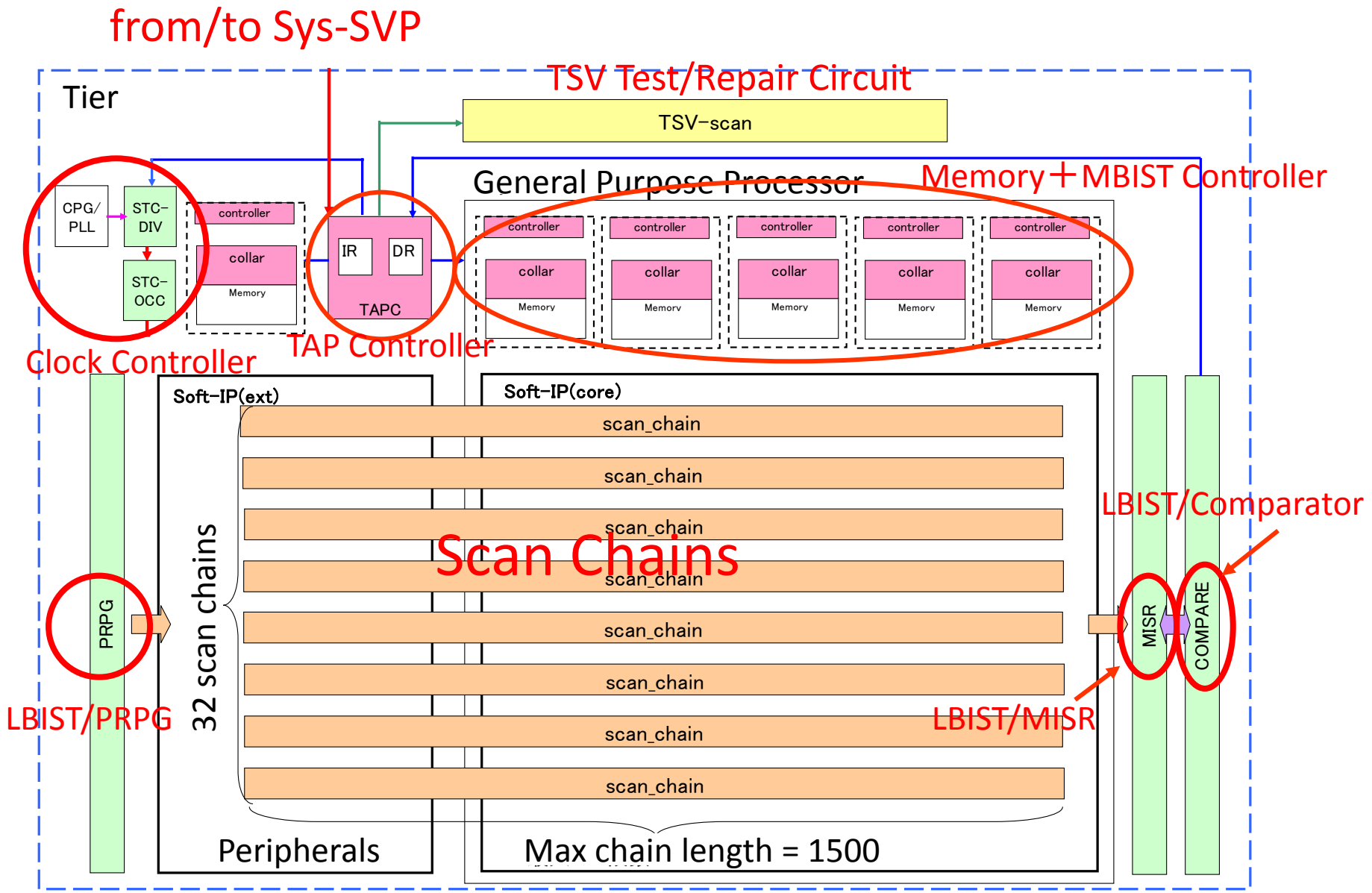
3D-DfT Architecture - Test Wrapper per Die

- Based on IEEE 1149.1
- Two Entry/Exit Points per Die:
  - Pre-Bond : Extra Probe Pads
  - Post-Bond: Extra TSVs

New 3D VLSI DfT Architecture for Online Self-Test of Dies Based on IEEE 1149.1.



Tier BIST Dynamically Controlled by System-Level SVP



Redundancy for Through Si Vias (TSVs)

		No Repair	Multiplexed TSV		With TSV Repair	
			m: multiplicity		n signals : r redundant TSVs	
			2	4	4:2	16:4
Area		+0%	+100%	+300%	+50%	+25%
Capacity		+0%	+100%	+300%	+0%	+0%
Switches/Sig		0	0	0	3	5
TSV Group Yield (n TSVs)		$(R_{TSV})^n$	$(1-(1-R_{TSV})^m)^n$		$\sum_{i=n}^{n+r}\binom{n+r}{i}R_{TSV}{}^i(1-R_{TSV})^{n+r-i}$	
Assembly Yield *	2,000	$1.9\times10^{-7}\%$	81.87%	99.99%	99.03%	99.98%
	5,000	$1.5\times10^{-20}\%$	60.65%	99.99%	97.59%	99.96%
	10,000	$2.2\times10^{-42}\%$	36.79%	99.99%	95.23%	99.91%
	20,000	$5.1\times10^{-86}\%$	13.53%	99.98%	90.69%	99.83%

Samsung (ISSCC 2009)

This Work

*assumed $R_{TSV} = 0.99$

Approach for HW-SVP

- Establishing a self-repair scheme for HW-SVP
  - Soft-error recovery using dynamic reconfiguration
    - Designing recovery controller and Scrubbing controller
    - Designing fault-tolerant system using TMR scheme

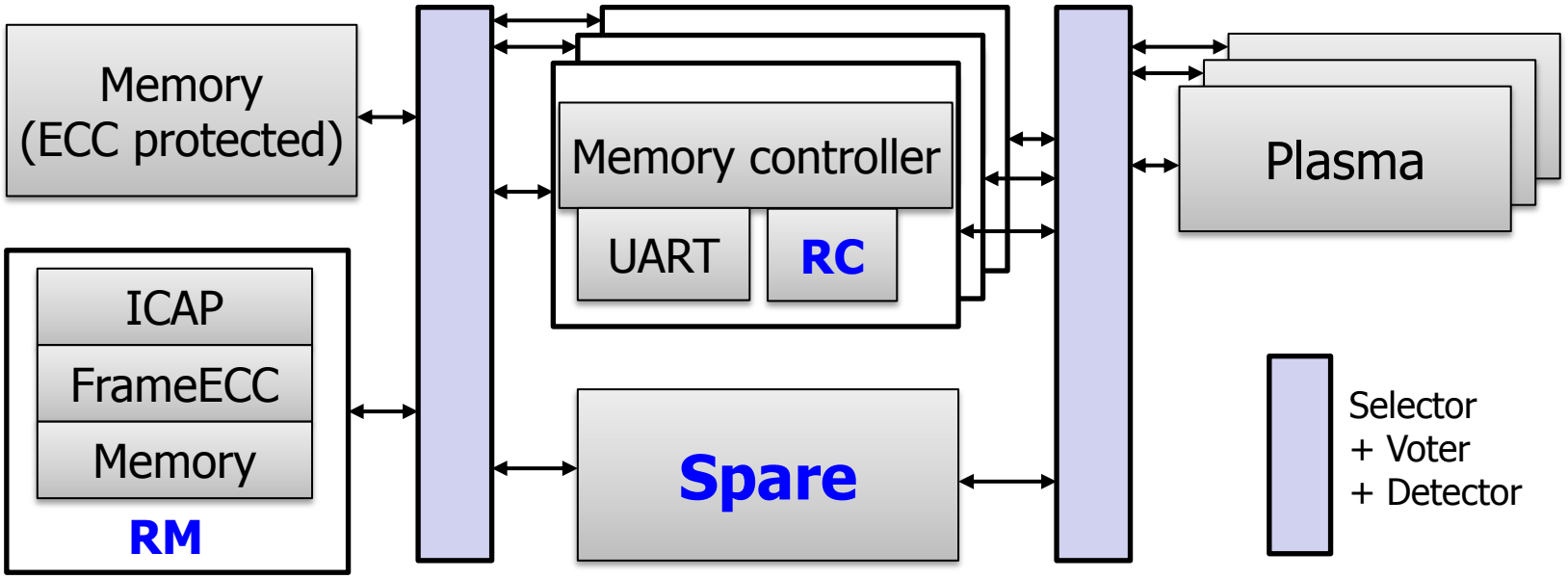
    Developing Evaluation system to evaluate soft-error tolerability
  - Hard-error avoidance using partial reconfiguration
    - Relocating partial reconfiguration bitstream (PRB)
    - Designing TMR scheme with Spare

    TMR : Triple Modular Redundancy

Self-repair scheme and Evaluation system

After Prof. T. Sueyoshi (Kumamoto Univ.)

System Configuration of HW-SVP



Implemented on：Xilinx Virtex-6 XC6VLX240T

- Triplicating processor core and peripheral modules
- Implementing RM, RC and Spare
  - RM and RC control recovery sequence
  - Spare is used for hard-error avoidance

RC : Recovery Controller　　RM : Recovery Module　　ICAP : Internal Configuration Access Port

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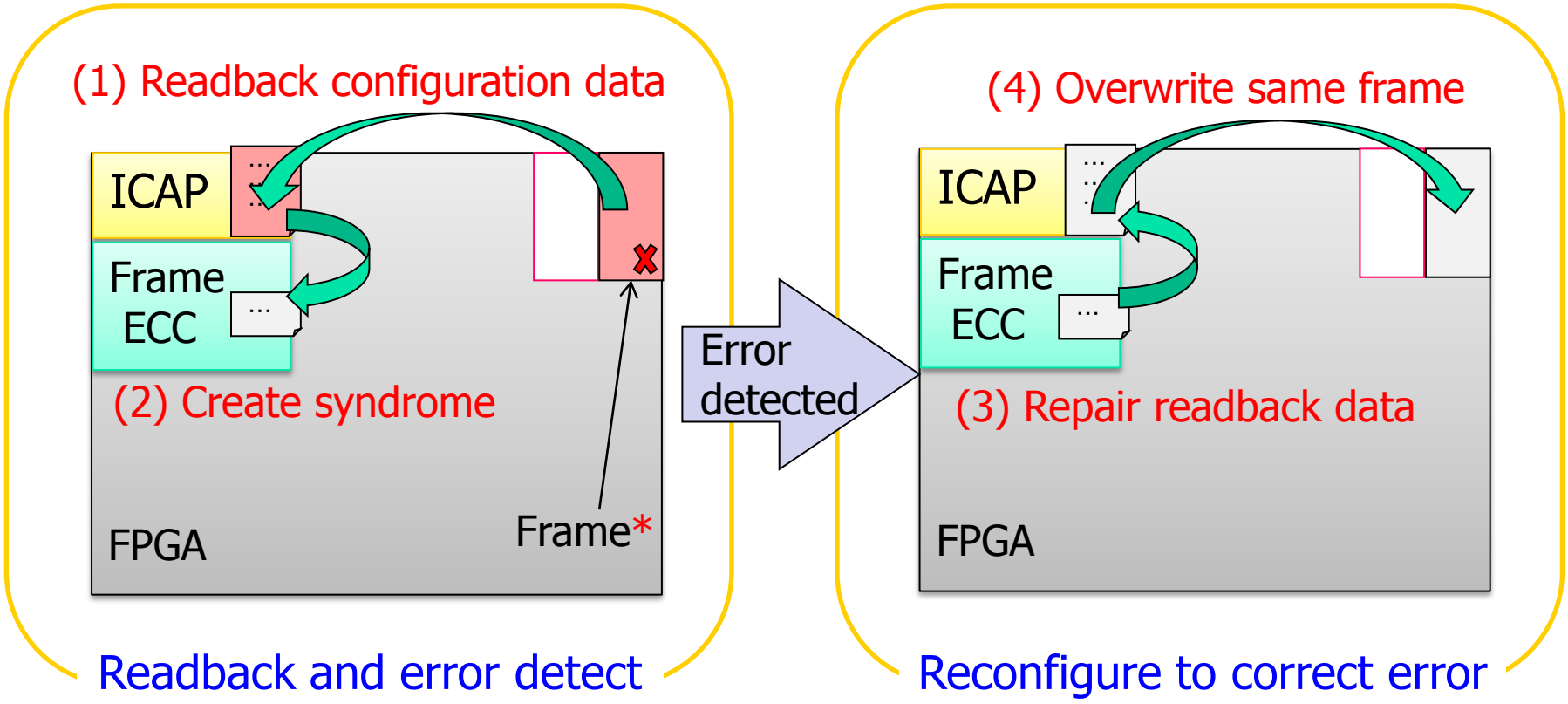
Soft-Error Recovery in HW-SVP

- Readback and Overwrite reconfiguration (Scrubbing)



Apply these sequence for all frame

* Frame : Minimum unit of reconfiguration
(1 frame = 2,592bit on Virtex-6)

ICAP : Internal Configuration Access Port

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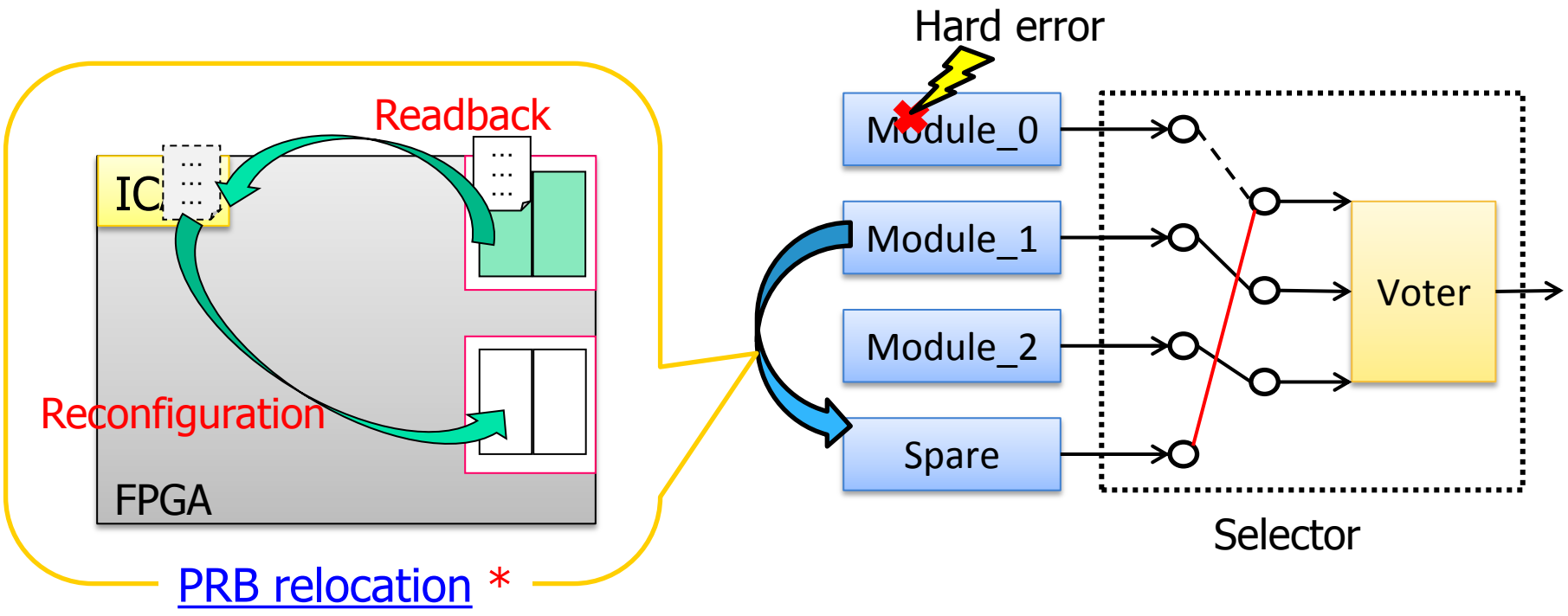
Hard-Error Recovery in HW-SVP

- Relocate PRB and separate a broken module



Implementing a copy of Module on Spare
to reconstruct TMR configuration

* This is realized by uniforming inner configuration of PR region (reported on Dec. 2011)

After Prof. T. Sueyoshi (Kumamoto Univ.)