



Development of Dependable Network-on-Chip Platform

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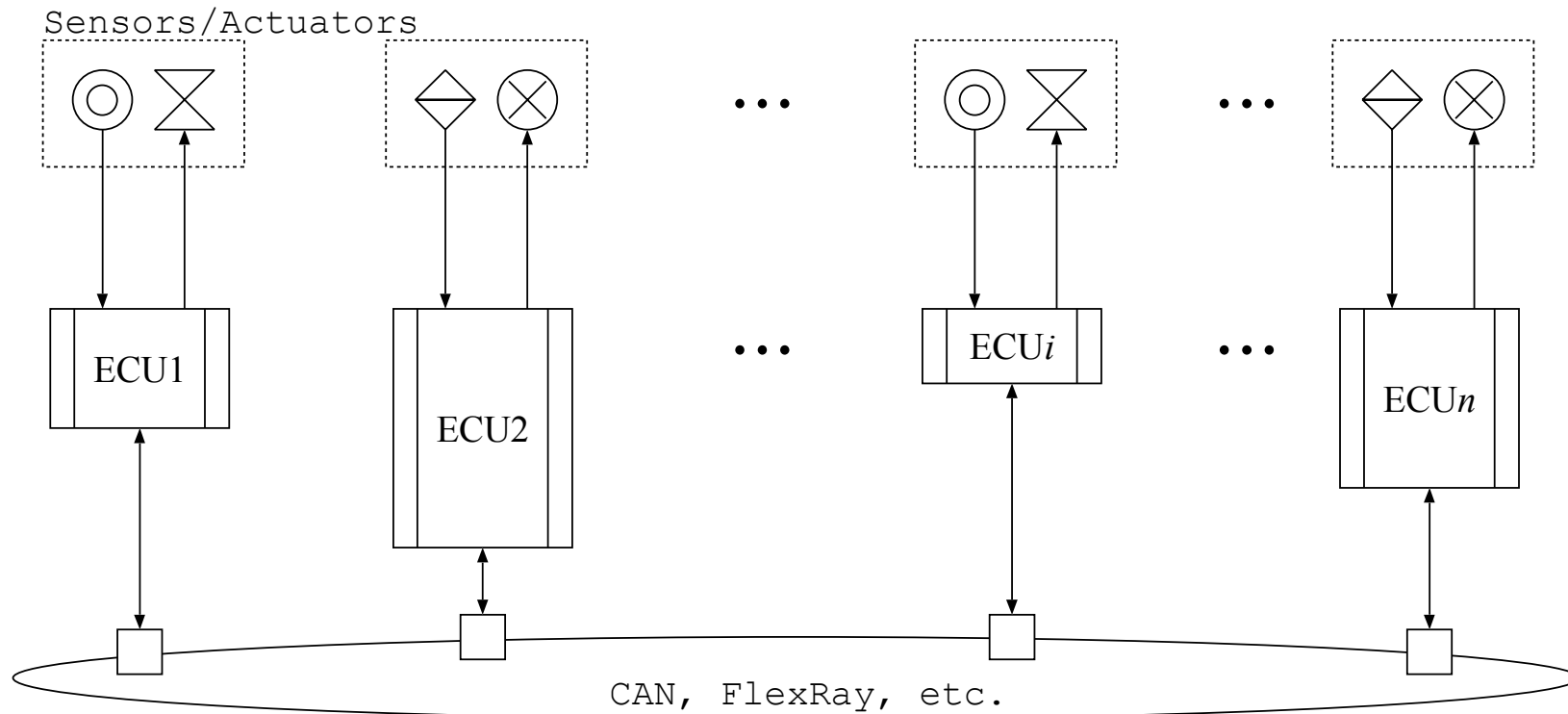
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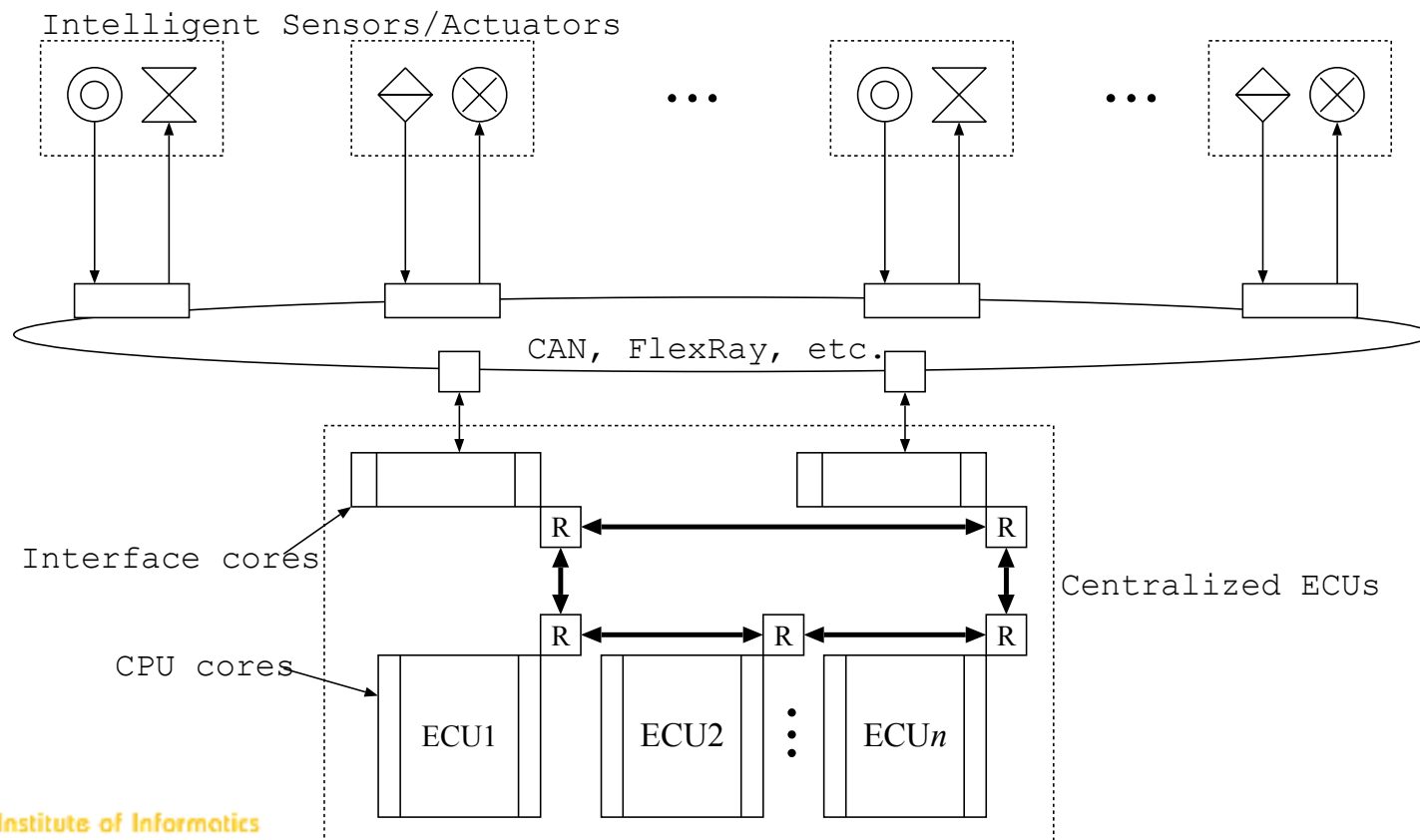
Backgrounds

- ◆ Recent cars are equipped with many ECUs
 - Conventional ECU configuration



Backgrounds

- ◆ Recent cars are equipped with many ECUs
 - Centralized ECU approach

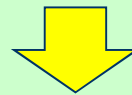


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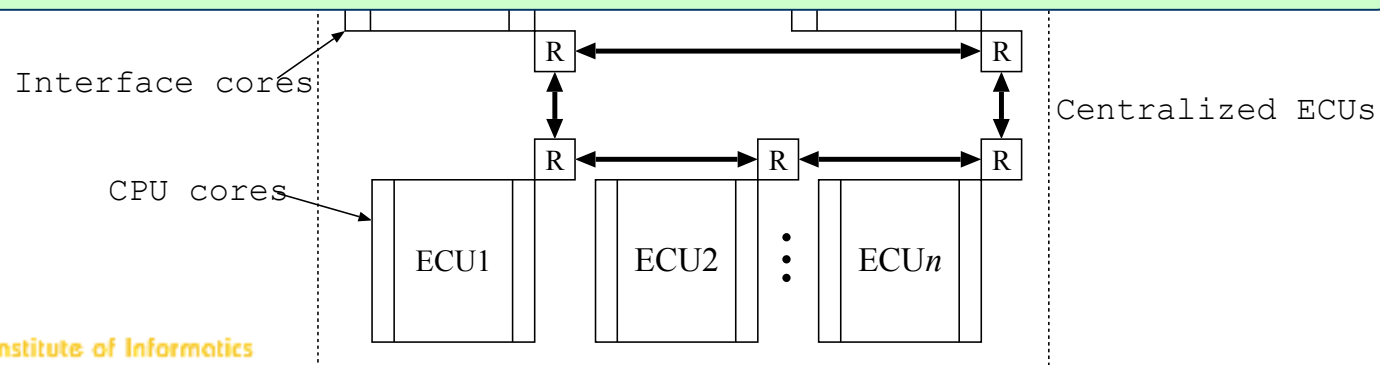
Intelligent Sensors/Actuators

Any ECU can access any sensors/actuators



ECUs efficiently used by balancing loads

Tasks continuously executed even if some ECUs become faulty
(i.e., faulty ECU does not result in malfunction of its specific functions)



Backgrounds

- ◆ Centralized ECU approach
 - NoC (Network-on-Chip) based
 - Some European projects
 - ◆ Recomp: Reduced certification costs for trusted multi-core platforms. <http://atc.ugr.es/recomp/>.
 - ◆ Race: Robust and reliable automotive computing environment for future ecars. <http://projekt-race.de/>.
 - Multi-Chip NoC based [Yoneda, et al. PRDC2012]
 - Multiple NoCs are connected via off-chip links
 - ◆ On-chip networks seamlessly extended to multi-chip networks
 - Advantages
 - ◆ Cost-effective : small NoC chips are cheap, and various sizes of configuration are possible (without developing different sizes of NoCs)
 - ◆ Chip-level redundancy : tolerate a chip fault

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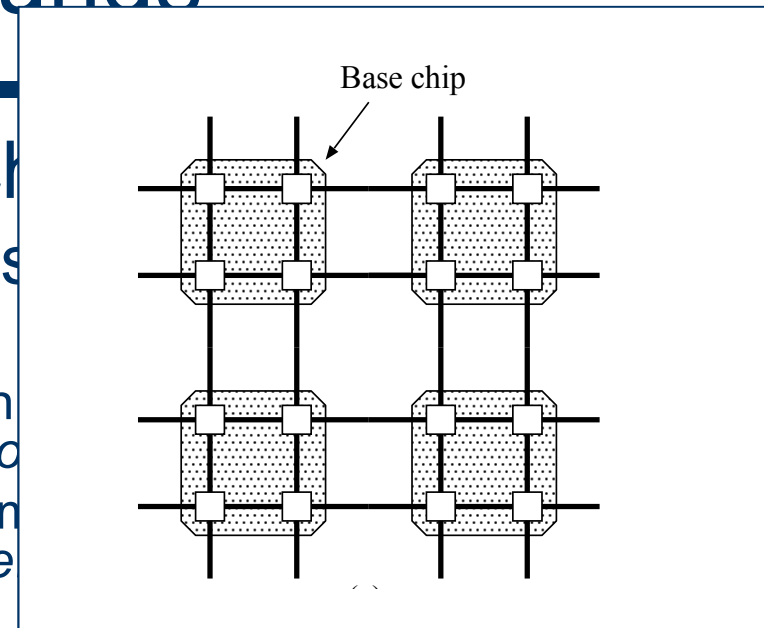
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Our Project

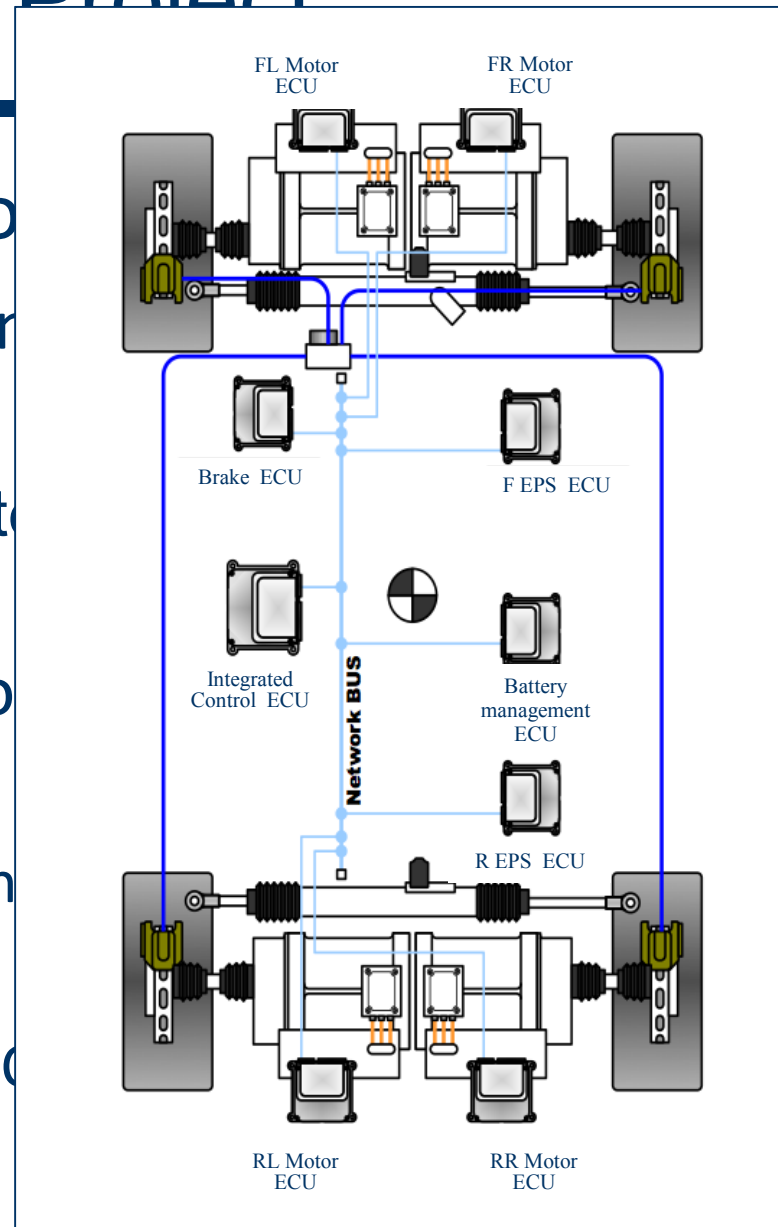
- ◆ Hardware platform
 - Multi-Chip NoC
 - Dependable, adaptive, deadlock-free routing
 - Efficient inter-chip communication technology
 - Evaluation board
- ◆ Task execution
 - Pair & Swap
 - SmartCore
- ◆ Task allocation
 - Redundant allocation, redundant scheduling

Our Project

- ◆ Automotive Application
 - Integrated attitude control system for a four-wheel drive car
 - Torque, brake, and steering control of 4 wheels performed by ECUs
 - Highly cooperative process needed by each ECU
 - Integrated Control ECU
 - 2 Electric Power Steering Control ECUs
 - Brake Control ECU
 - Battery Management ECU

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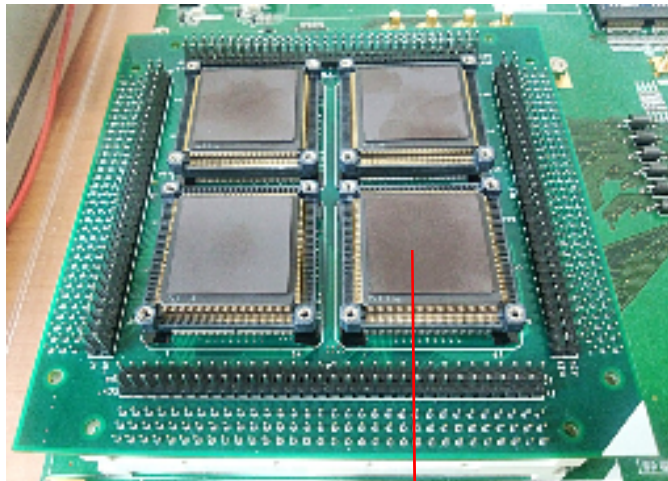


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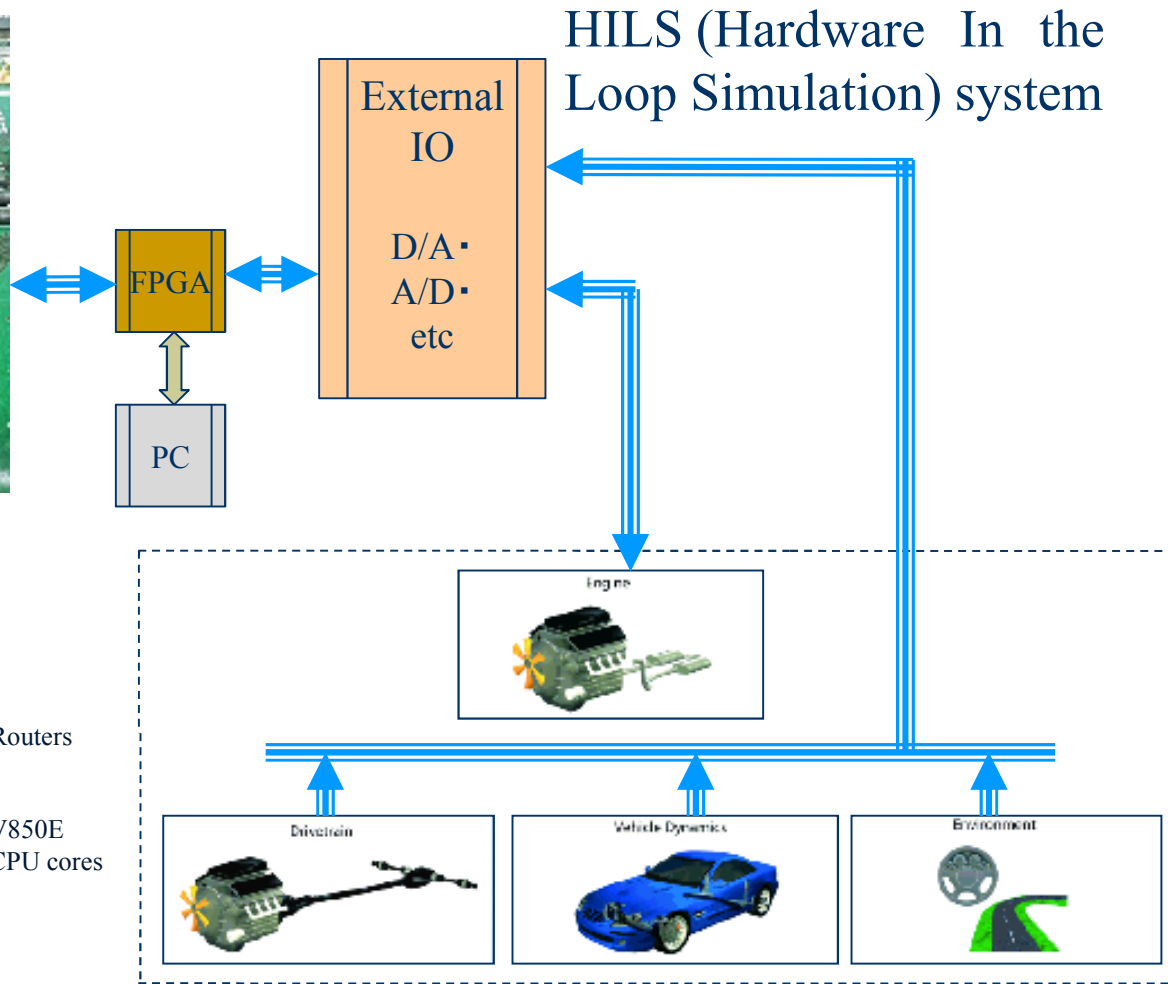
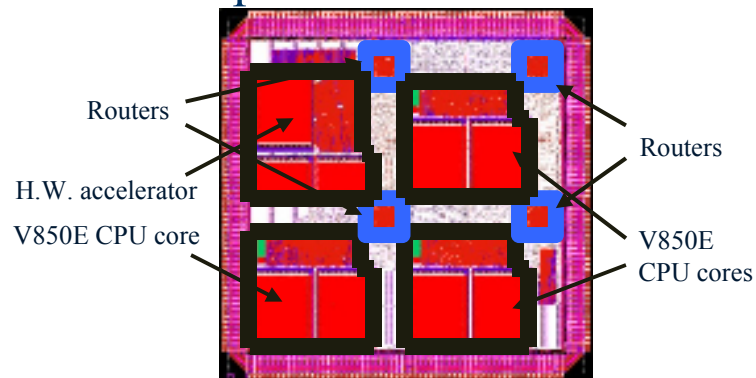
- ◆ Characteristics of this application
 - Stopping control is very dangerous
 - Higher availability is required

Experimental system

Base chip × 4



Base chip



Ongoing work

- ◆ Evaluation kit
 - NoC implementation
 - 4 Multi-Chip ASICs
 - Vertex7(XC7VLX690T)
 - HILS interface
 - Pseudo HIL-plant models (executable on PC)
 - Redundant task allocation tool
 - Input: (Simplex) Simulink model for application
 - Output: Executable codes for redundant cores