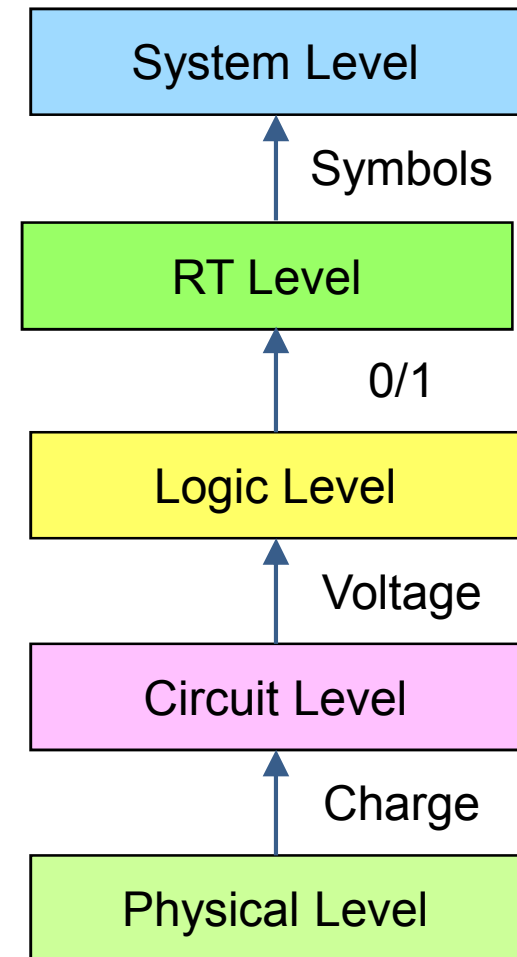


# Modeling, Detection, Correction and Recovery Techniques for Unified Dependable Design

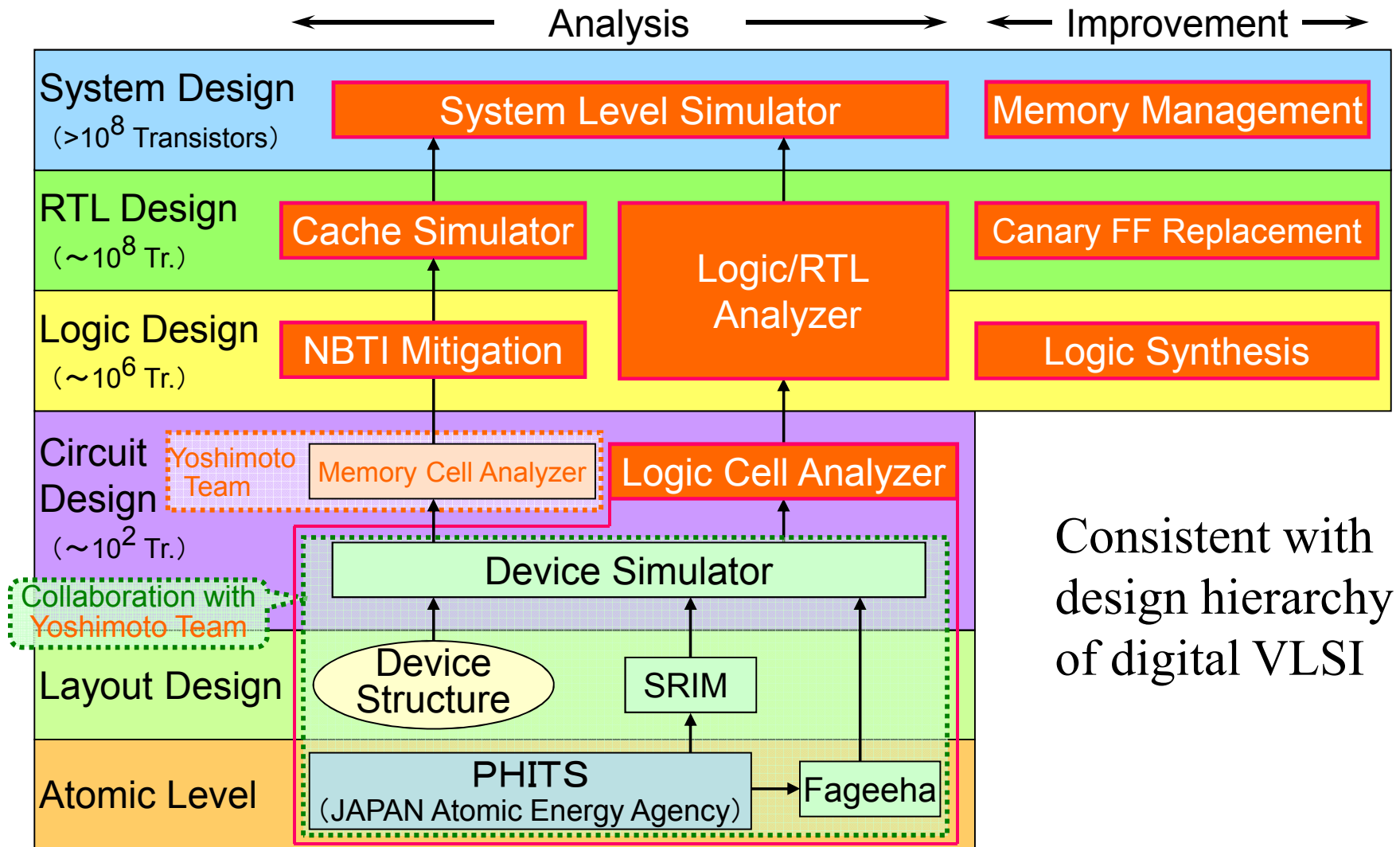
Hiroto Yasuura  
Kyushu University

# Analysis of Dependability in VLSI Design

- Analysis techniques of dependability for hierarchical VLSI system design are required.
- Error in the lower level should be modeled in different signals in the upper level.
- In most conventional researches, error models are supposed independently and dependability is analyzed in each level.
- We developed a tool chain, which can analyze dependability from the results in the lower level for soft error of digital VLSI.
  - Techniques for transfer error model from analyzed results in the lower level
  - Reduction algorithms of the computation time of analysis against the rapid increase of the number of transistors in the upper levels
- We also developed other technologies for dependable VLSI design
  - Resilient design by Canary FFs
  - Trade-off between design for testability and security

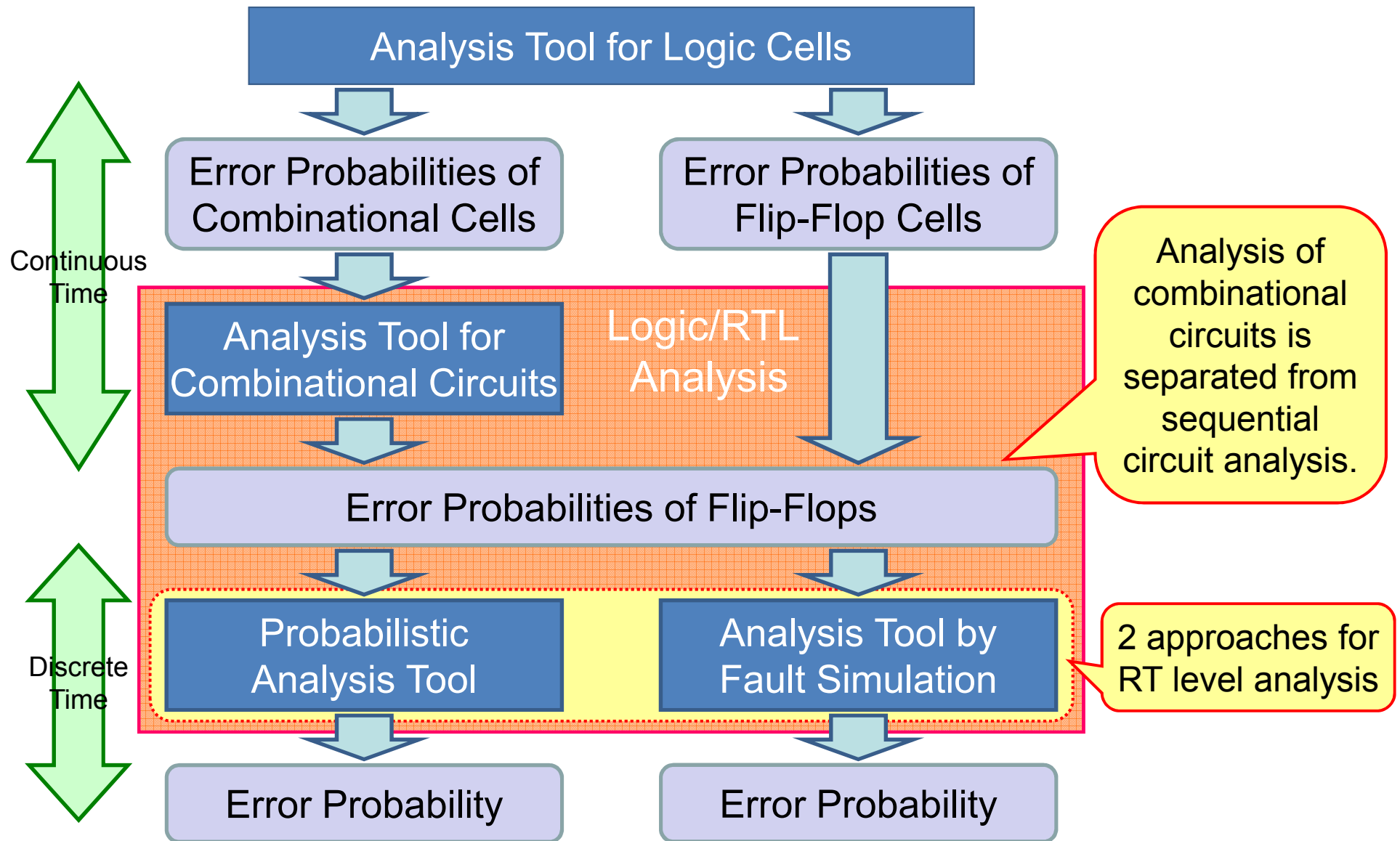


# Tool Chain for Soft Error Tolerance

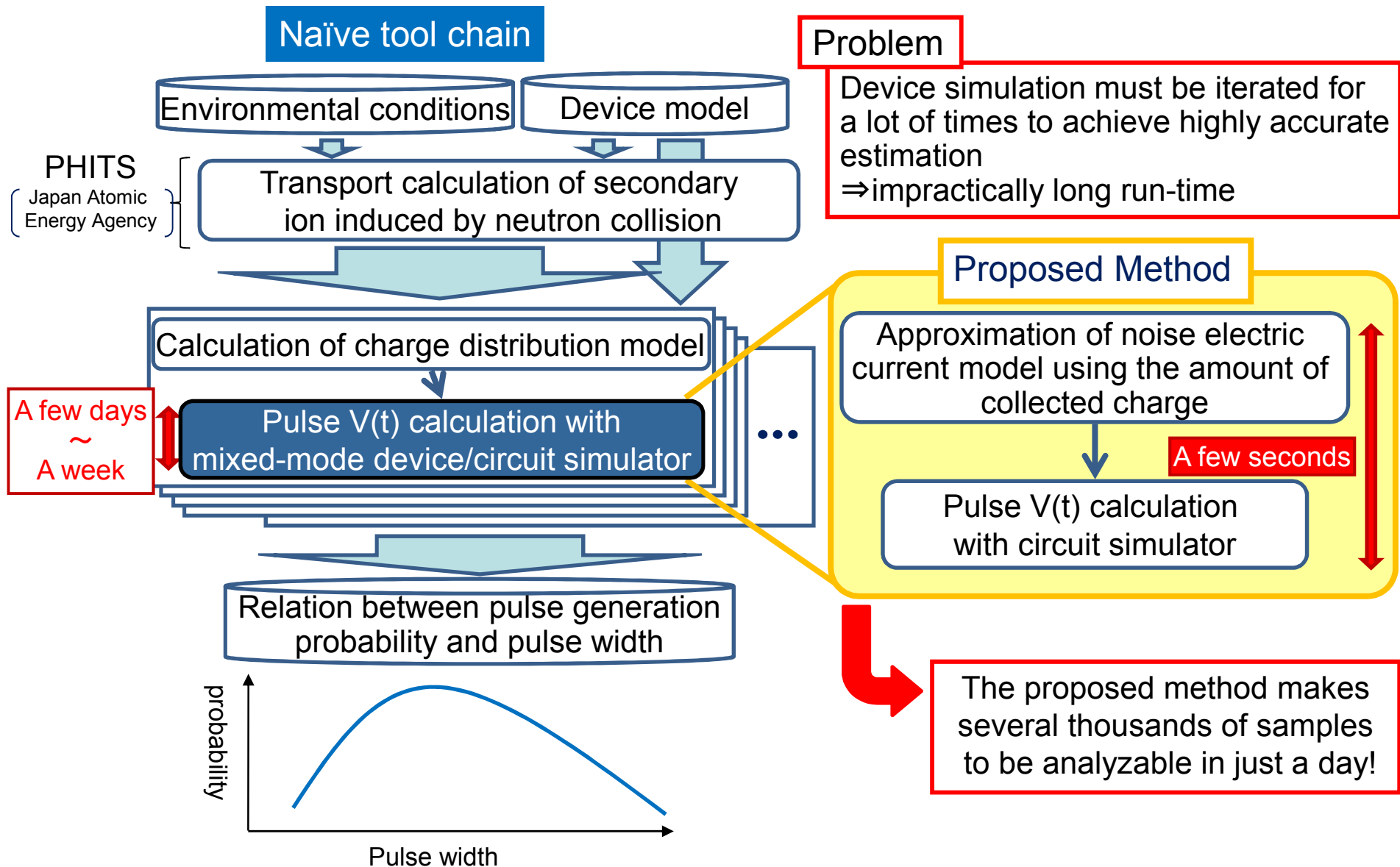


Consistent with design hierarchy of digital VLSI

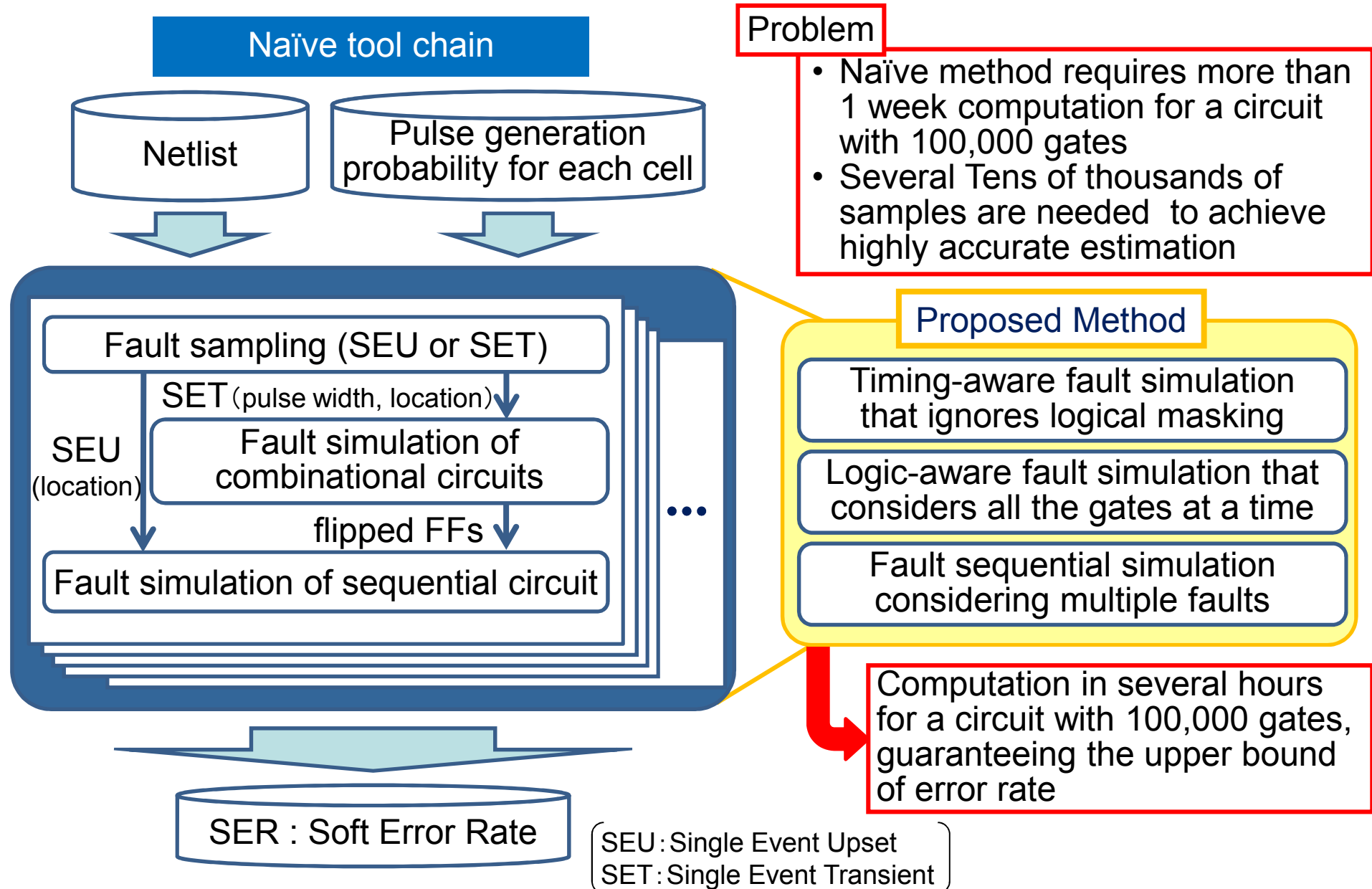
# Error Models and Analysis Tools



# Analysis Tool for Logic Cells

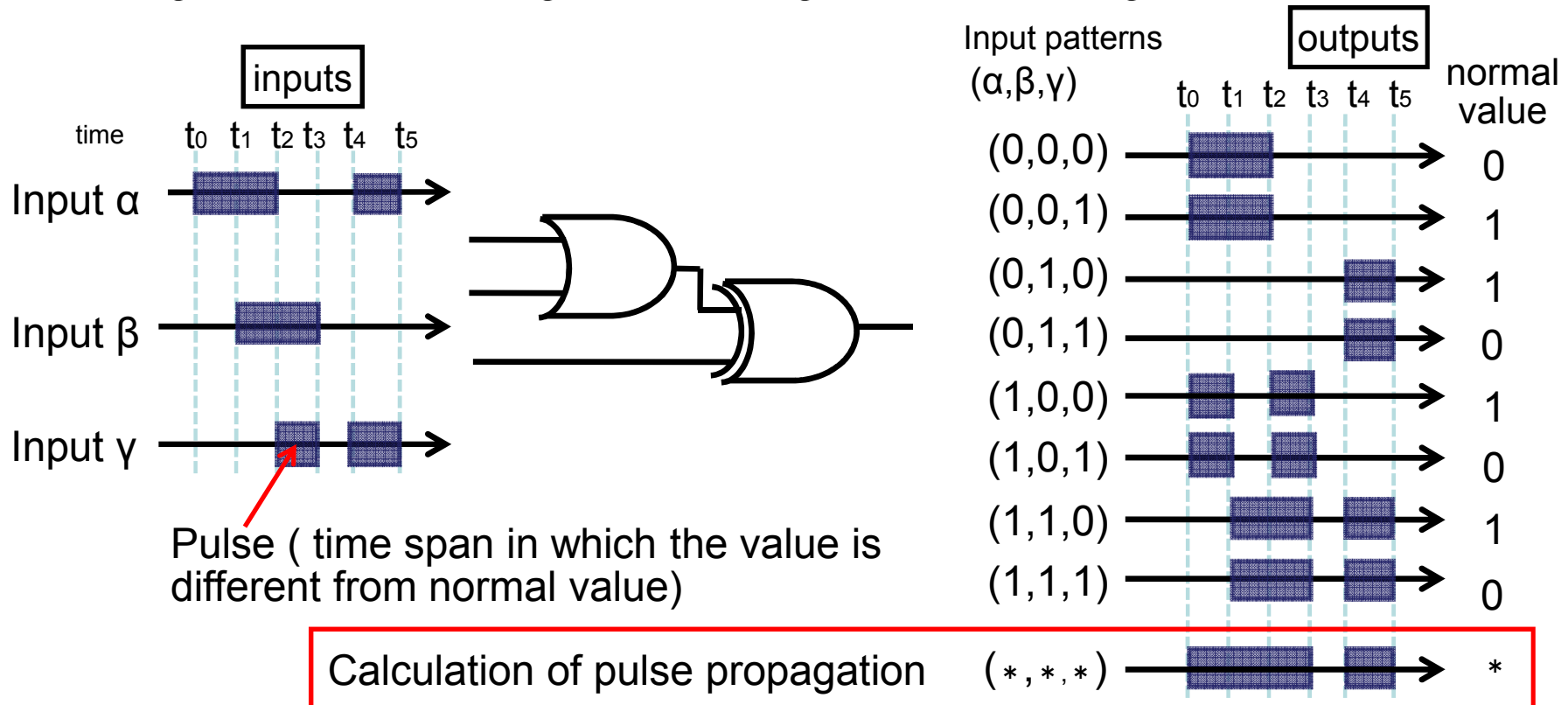


# Analysis Tool for Logic/RTL Circuits

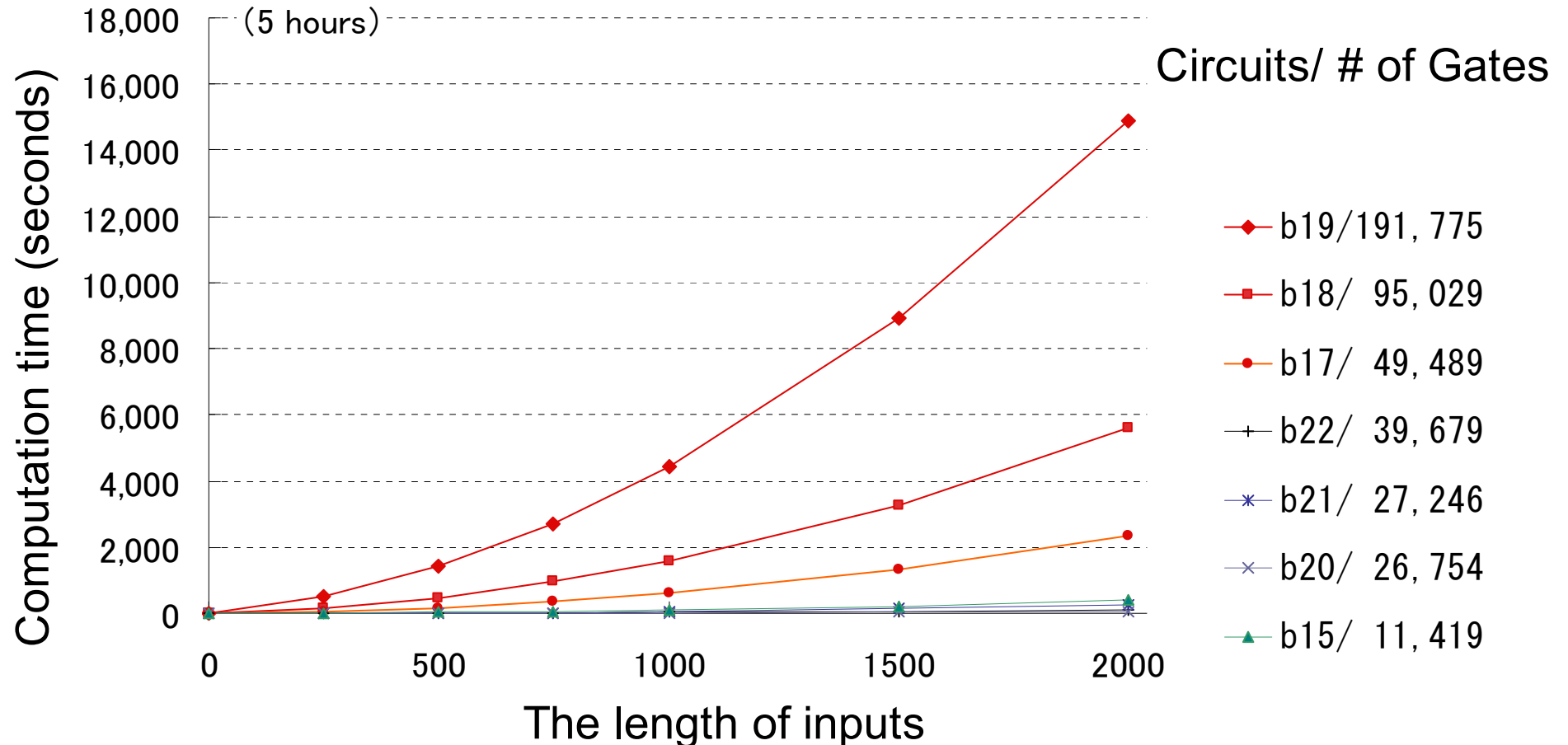


# Timing-Aware Fault Simulation

- Analysis of propagation of a pulse caused at a gate to flip flops and/or primary output terminals considering its pulse width and timing
- Calculate the upper bound of the pulse width and estimate probability of which the pulse is latched onto the flip flops
  - Consider the variation of pulse width on the propagation paths
  - Ignore effects of logical masking and re-convergence



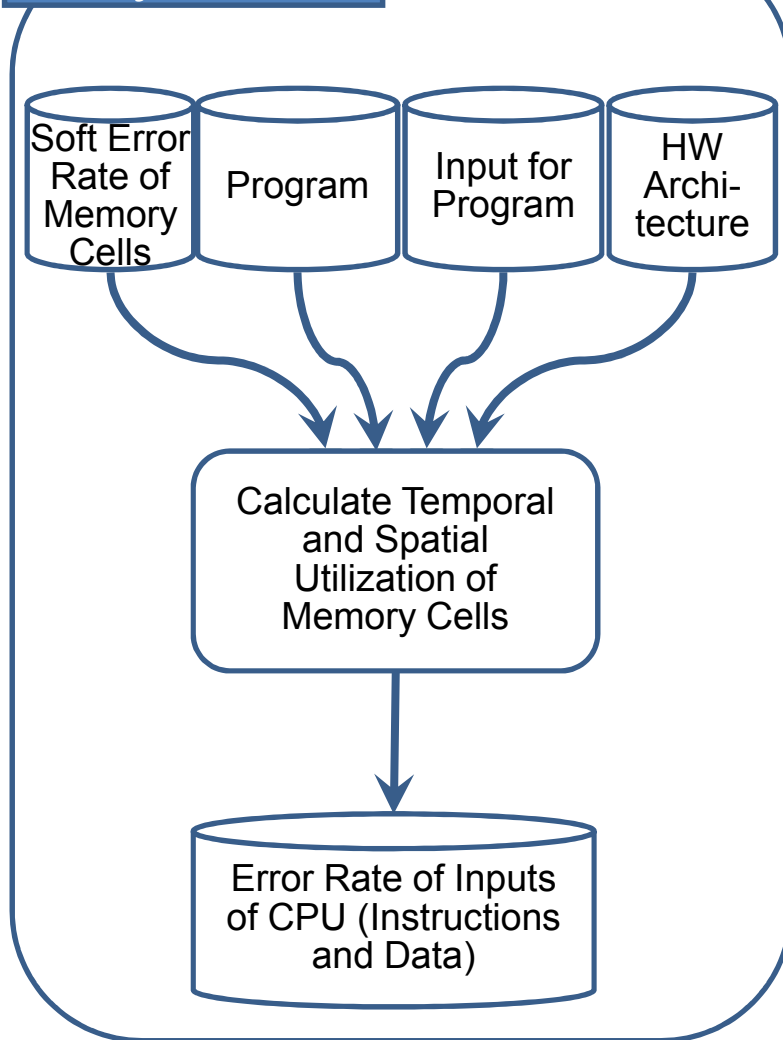
# Computation Time of Accelerated Fault Simulation



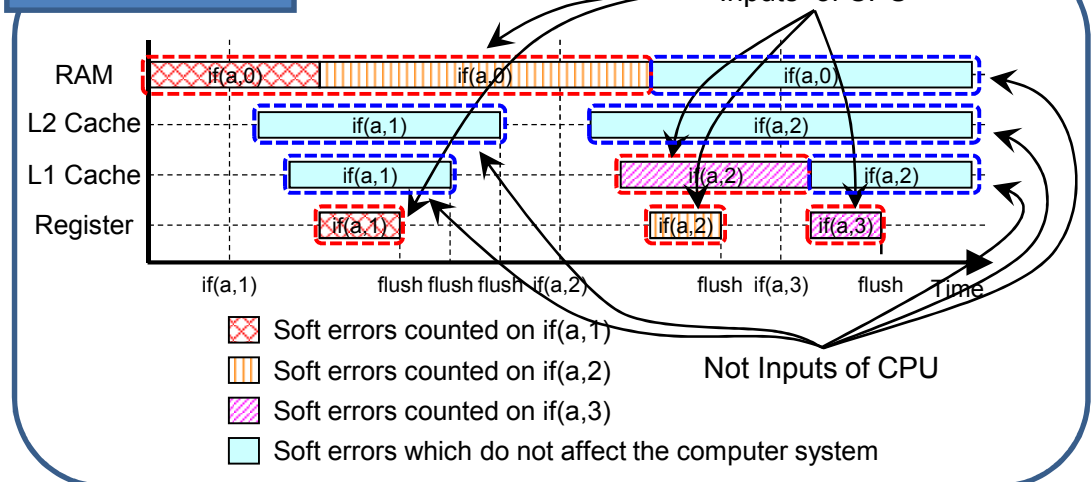


# Memory System Simulator

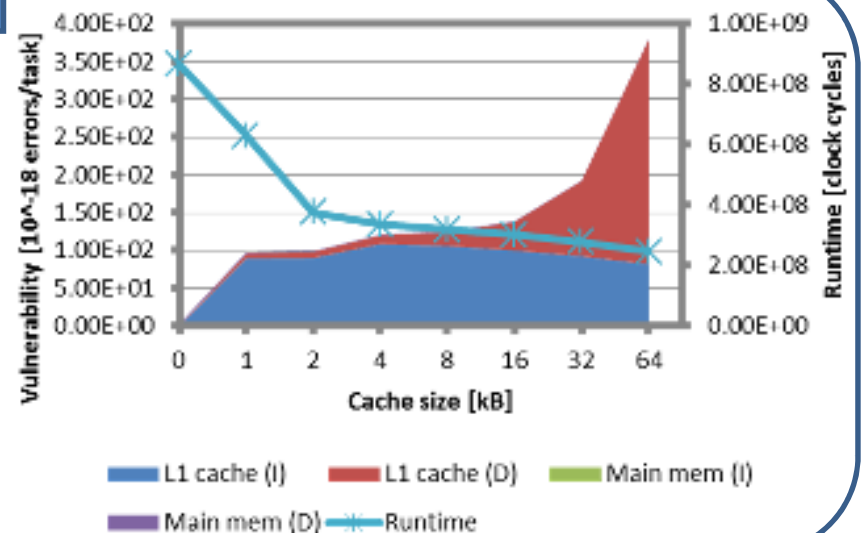
## Analysis Flow



## Evaluation



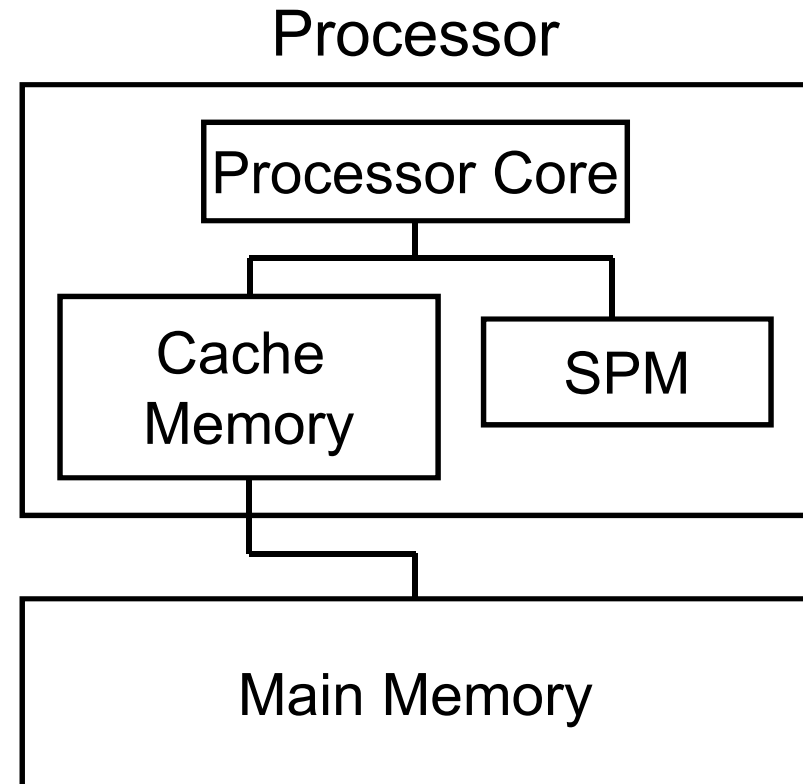
## Results



# Example: Highly Dependable Design of Embedded Systems Using a Scratch Pad Memory

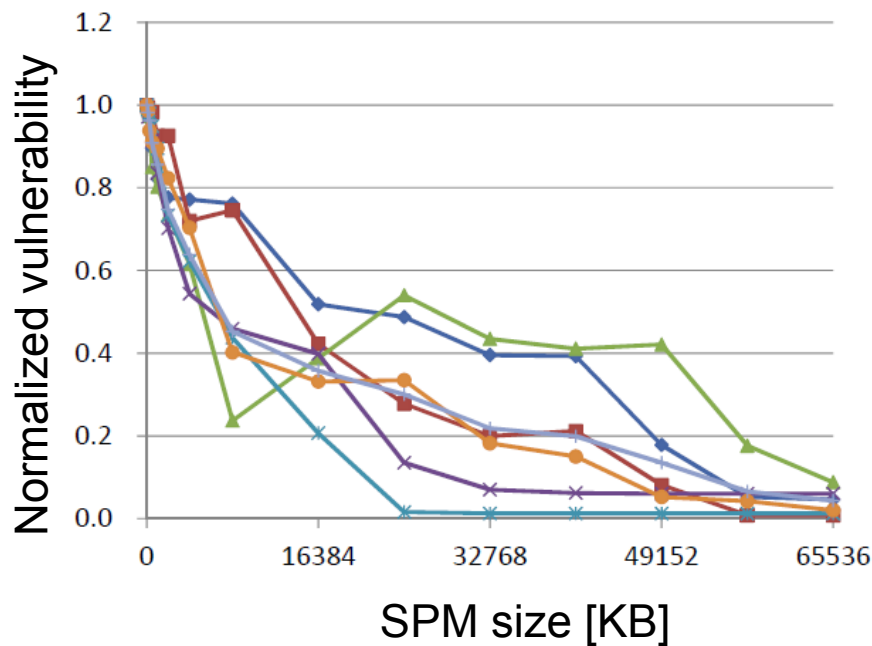
- No error correction in Cache Memory
- Error correction circuits in Scratch Pad Memory (SPM)

Improve dependability by allocation of program and data in SPM

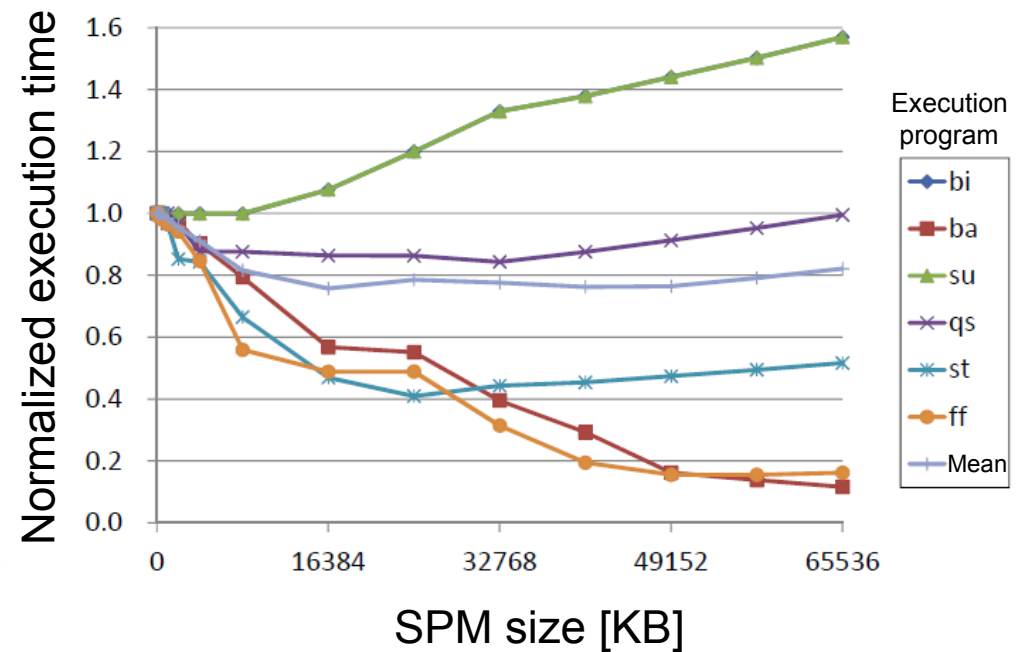


# Trade-off Analysis between SPM Size and Vulnerability (Inverse of Error Rate)

Vulnerability (cache size: 16 KB)



Execution time (cache size: 16 KB)



# Summary

1. Concept of Design Flow and Tool Chain for Dependable VLSI
  - Unified tool chain from physical phenomena to system level for estimation of dependability compatible with hierarchical design flow
  - Three practical problems: Soft Error, Timing Error and Security
2. Soft Error Caused by Neutron
  - Analysis tools for logic cells, combinational circuits and sequential circuits (logic and register transfer levels)
  - Memory architecture simulator and trade-off analysis
3. Timing Errors by Fluctuation of Manufacturing
  - Introduction of Canary Flip Flops for reducing design margin
  - Improvement of static noise margin of SRAM
4. Design for Security
  - Trade-off analysis between testability and security