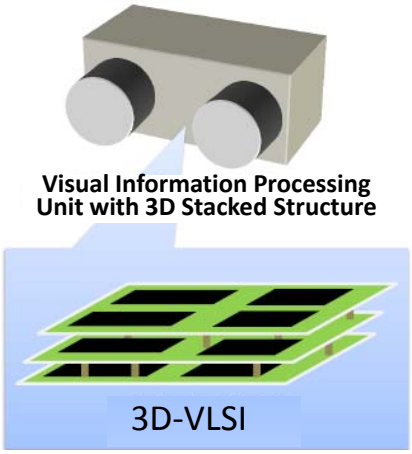
JST International Symposium on
Dependable VLSI Systems 2012

Development of 3D-VLSI System with Self-Test and Self-Repair Function

Mitsumasa Koyanagi , Tohoku University
Hiroaki Kobayashi, Tohoku University
Takafumi Aoki, Tohoku University
Toshinori Sueyoshi, Kumamoto University
Tadashi Kamada, DENSO Corporation
Makoto Motoyoshi, Tohoku-MicroTec

1

Setting Target for High Performance Image Processing System to Guarantee Safety in Automobile Driving Assist



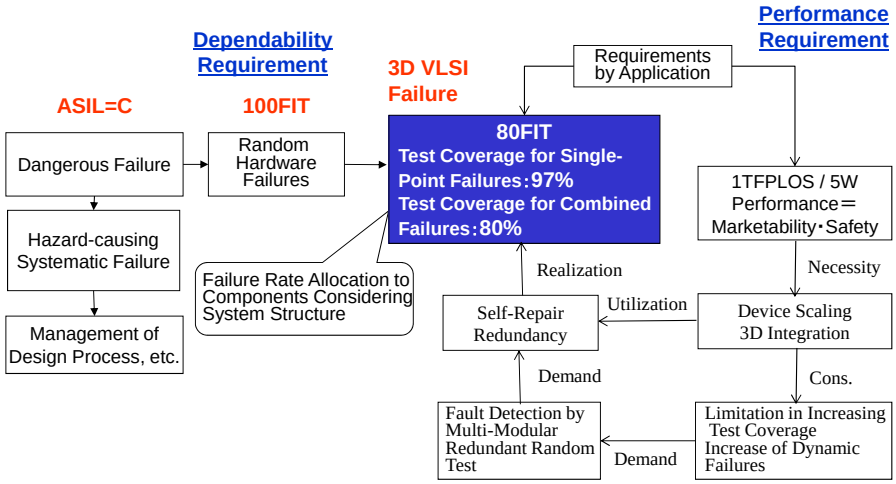
- Number of camera: 2
- Measuring distance: 0～100m
- Base line length: 12cm
- Focus length: 6.5cm
- Pixel resolution: SXGA
- Window size: 48 pixels x 31 lines
- Reconfiguration points: 30,000
- Matching accuracy: 1/20 Pixel
- Z Axis resolution
  (Measuring distance accuracy):
  80cm resolution at 50m ahead
  3m resolution at 100m ahead
- Calculating ability : ～1TFLOPS

2

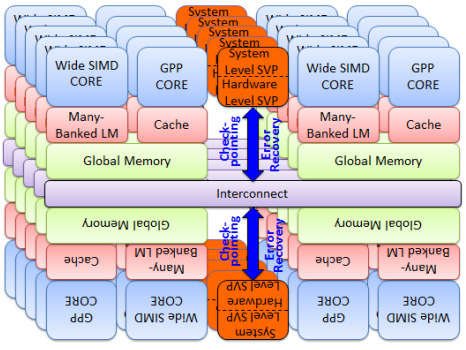
Application of 3D VLSI to Image Processing VLSI for Automobile

Relation between Requirements by Application and Various Technologies

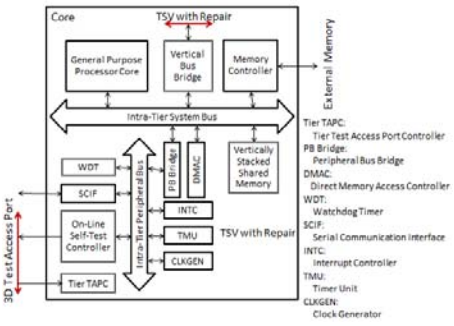
Target : ISO 26262 ASIL=C



Architecture of 3D-DVLSI System



Configuration of 3D stacked multicore processor

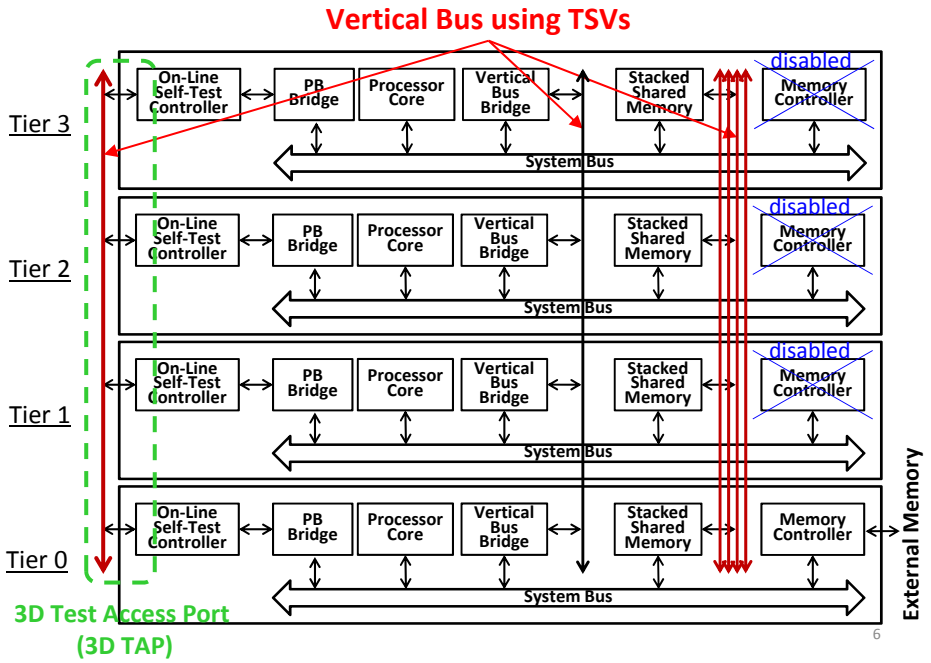


Block diagram of a processor core

Purpose for Fabrication of Prototype 3D-Stacked Graphics Processor

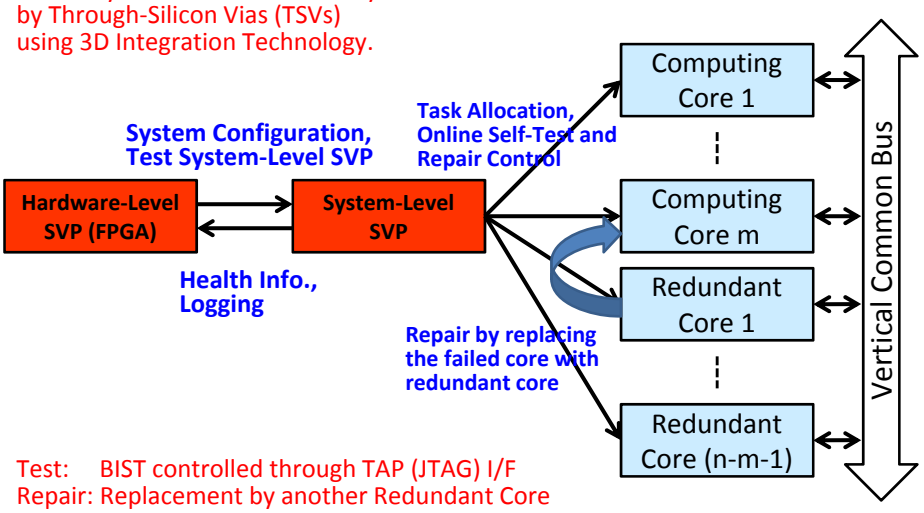
- Evaluation of self-test control
  - BIST operation control
- Verification of design methodology for TSV circuits
  - DFT for TSV
    - Electrical conduction pass test for each TSV
  - TSV repair method
    - Arrangement of repair TSVs for a group of signal TSVs
    - Replacement of failure TSVs by repair TSVs which pass electrical conduction test.
- Integration of functional blocks by TSVs
  - Vertical buses/ Vertical bus bridges
  - Integration of 3D shared memory
    - Maintaining of consistency
      - Maintaining consistency by updating memory contents at appropriate intervals using memory-update vertical buses
      - Memory access control by prohibiting memory access for updating memory area with each line.
      - Providing vertical buses for memory updating to each page
    - No memory replacement function as in cache memory

Block Diagram of 3D-DVLSI (e.g. 4 tiers)



Dependability Maintained by SVP

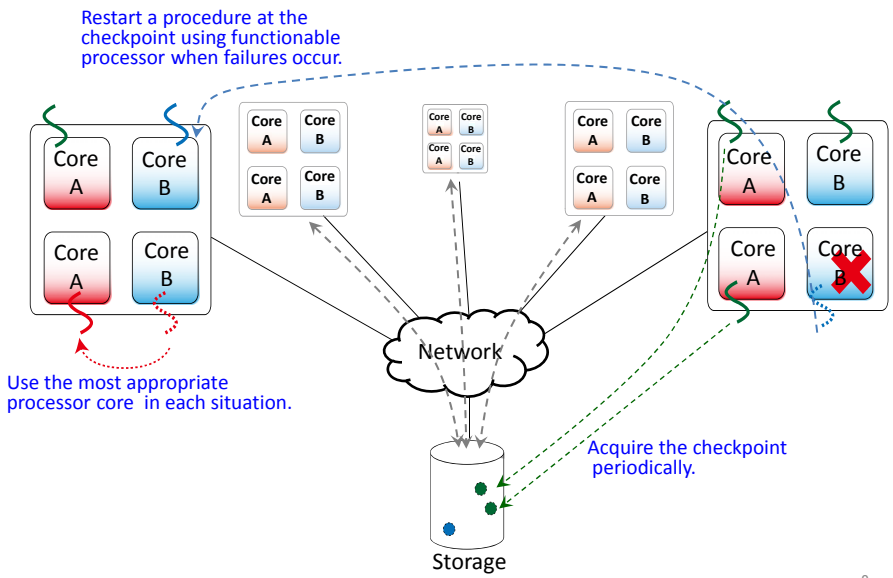
Vertically Stacked and Electrically Connected
by Through-Silicon Vias (TSVs)
using 3D Integration Technology.



Test: BIST controlled through TAP (JTAG) I/F
Repair: Replacement by another Redundant Core

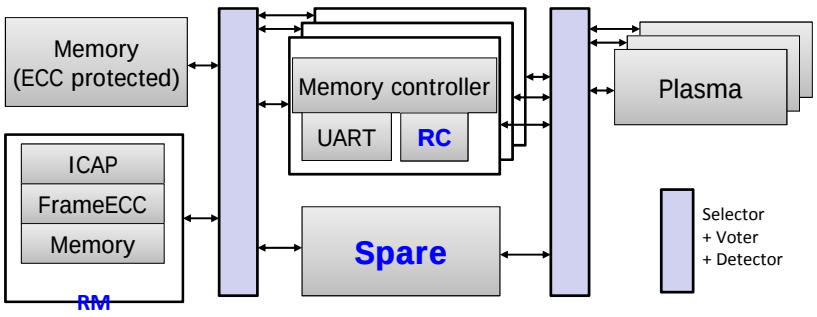
7

Check-Point and Restart Scheme for Heterogeneous Computing Platform



8

Dependable HW-SVP



Implemented on : Xilinx Virtex-6 XC6VLX240T

- Triplicating processor core and peripheral modules
- Implementing RM, RC and Spare
  - RM and RC control recovery sequence
  - Spare is used for hard-error avoidance

RC : Recovery Controller RM : Recovery Module ICAP : Internal Configuration Access Port

9

Summary

- We proposed a new dependable architecture for 3D-VLSI in which a system supervisor processor (Sys-SVP) controls self-test and self-repair circuits and a hardware system supervisor processor (HW-SVP) controls Sys-SVP to maintain dependability.
- We established a self-repair scheme with soft-error recovery using dynamic reconfiguration and hard-error avoidance using partial reconfiguration to guarantee dependability of HW-SVP.
- We employed a checkpoint and restart scheme to migrate all function in a failure processor layer to another processor layer to maintain dependability and proposed a new algorithm to dynamically perform self-test and migration to maintain performance in 3D stacked graphics processor.
- We introduced a new 3D DfT (Design for Test) architecture with on-line self-test using Sys-SVP through 3D TAP (test access port) based on IEEE 1149.1. into 3D stacked graphics processor to maintain dependability.
- We introduced redundancy methods to guarantee the reliability of TSVs (Through Si Vias) in 3D-VLSI.
- We evaluate power efficiency of 3D-VLSI assuming the application to image processing for automobile of obstacle detection using stereo vision with POC (Phase-Only Correlation)-based correspondence matching.

10