

Ultra Depedable VLSI by Collaboration of Formal Verifications and Architectural Technologies

CREST-DVLSI

- Fundamental Technologies for Dependable VLSI Systems -

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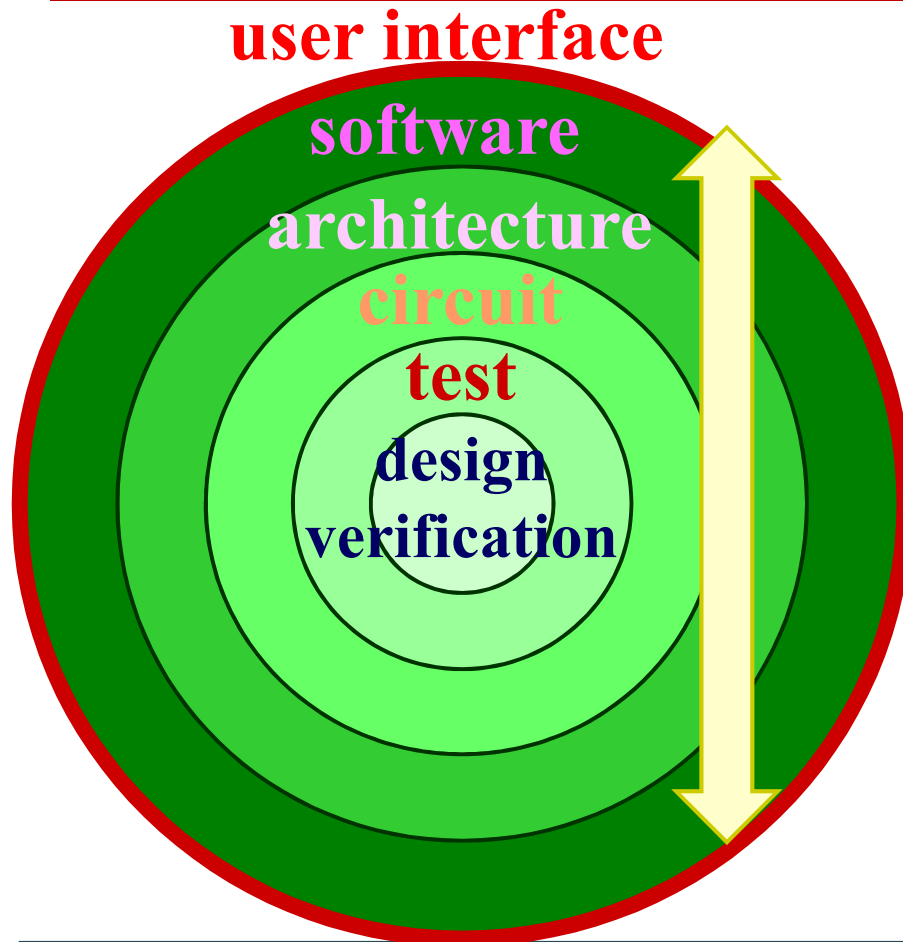
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Research Map: Dependability Layers

2



Research in each layer

- + Optimization among layers
- + Verification of the proposed architecture

Best Effort Design
Run Time Recovery

(1) Formal Verification

- Equivalence Checking Software
- Verifications by HW/SW Collaboration
- Collaborations of Bottom-up and Top-down Verification
- Synthesis, Verification and Optimization of Arithmetic Circuits
- Design Analysis and Support for Debugging

(2) Testing / Recovery at Testing

- Easy-to-Test Design
- Support for Post-Silicon Verification and Debugging
- Patchable HW

(3) Circuits

- Tolerating Timing Faults

(4) Architectures

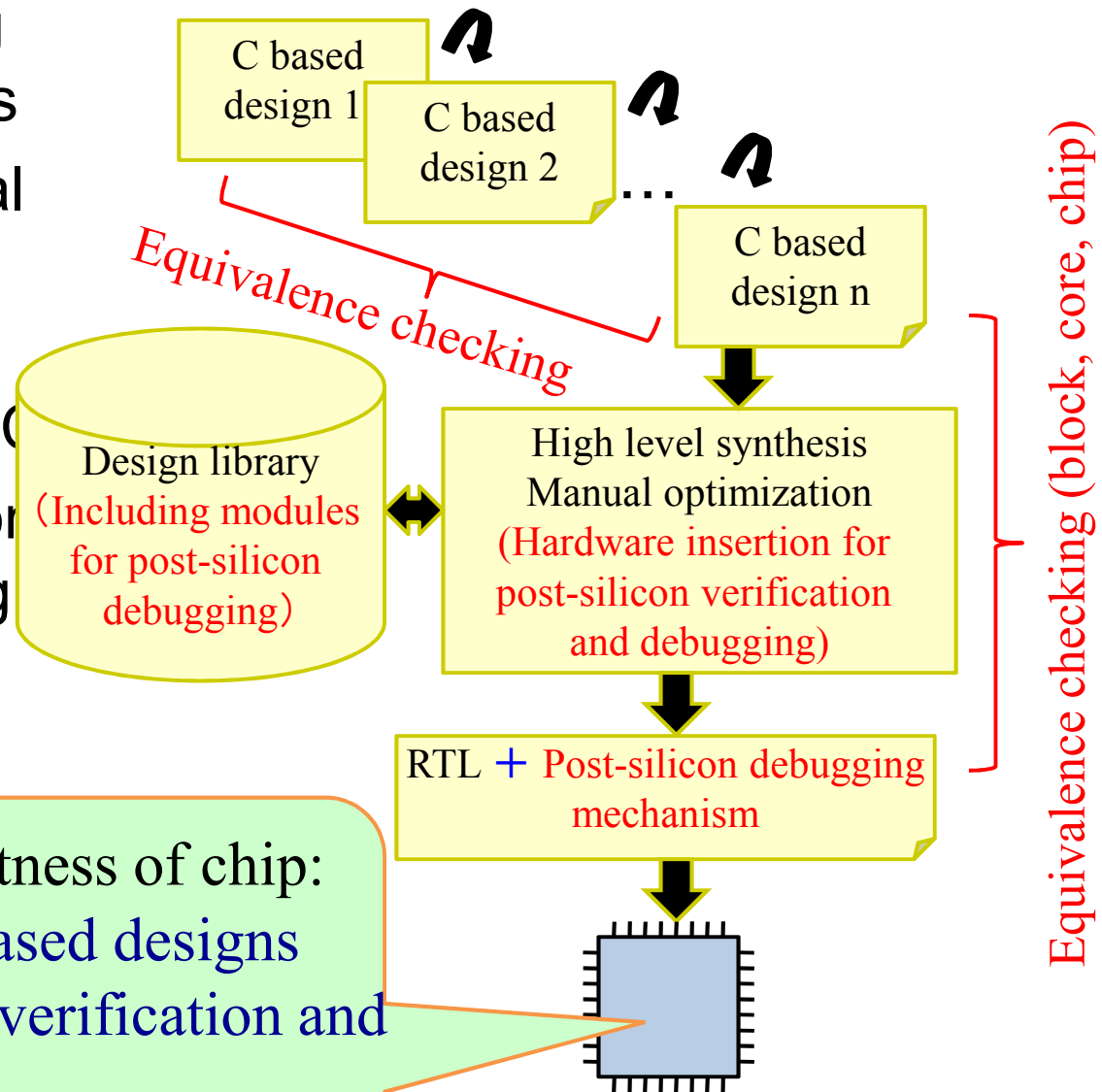
- Fault/Error Detection/Recovery
- FPGA with Permanent Error Recovery Mechanisms
- On Chip Multi-Function Routers
- Ultra Dependable Processor
- Ultra Dependable Many Cores

(5) Formal Verification of Proposed Architectures

(6) Optimization of Dependability Layers

Formal Verification and Debugging of VLSI ³

- Equivalence checking for design refinements
 - Developed a formal verifier, **FLEC**
 - Under industrial evaluation with NEC
- Support for post-silicon verification and debug
 - Developed **Patchable HW**

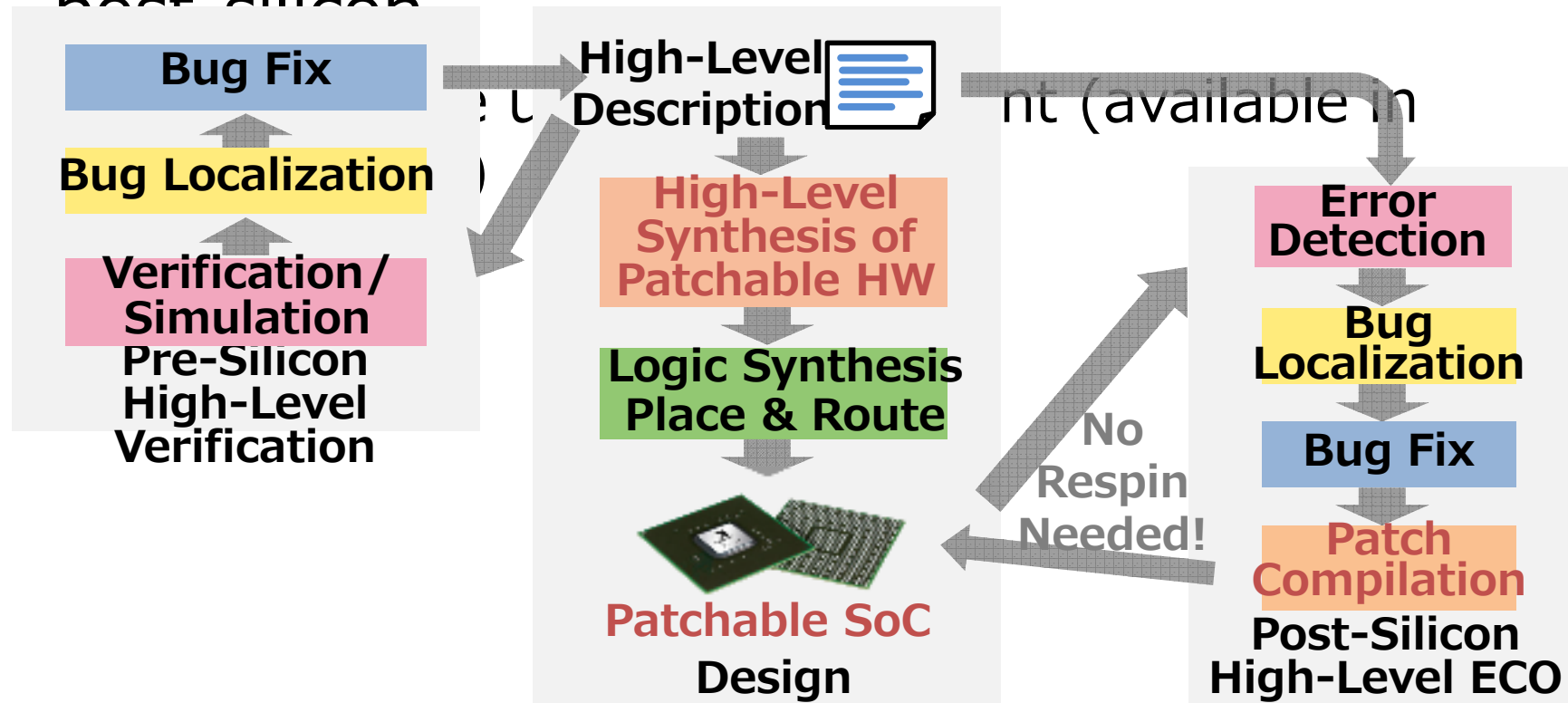


Guarantee the total correctness of chip:

- Behaves as original C based designs
- Post-silicon support for verification and debug (**Patchable HW**)

Patchable HW for post-silicon verification and debug

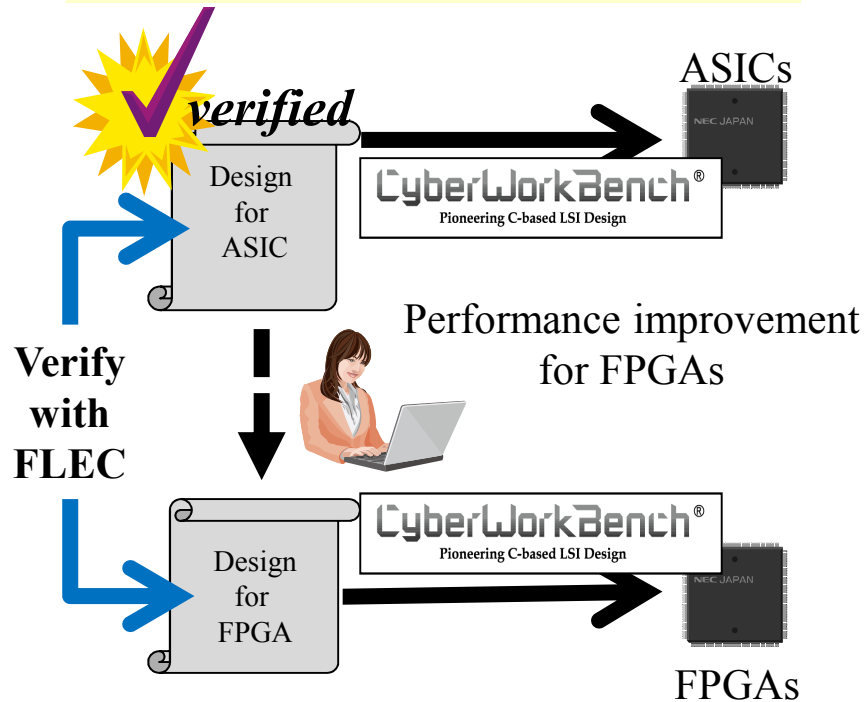
- Insert redundancy/programmability in design time
- Use them if something wrong happens at post-silicon



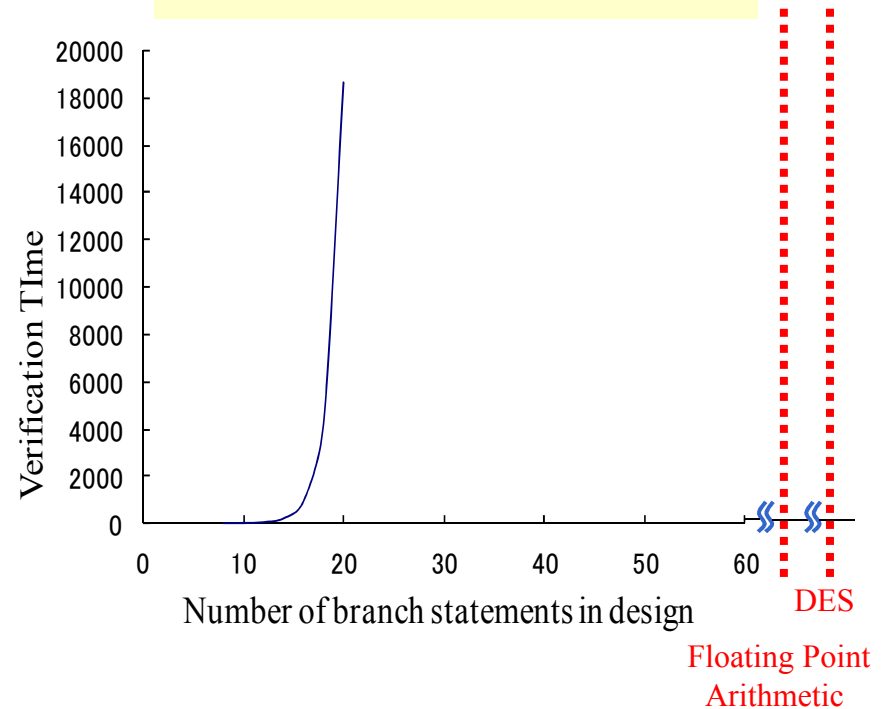
FLEC in an industrial design environment⁵

Target: Reduction of verification time required to ensure correctness after incremental improvement

Retargeting IPs designed for ASICs to FPGAs



Computation time explosion for industrial-level circuits

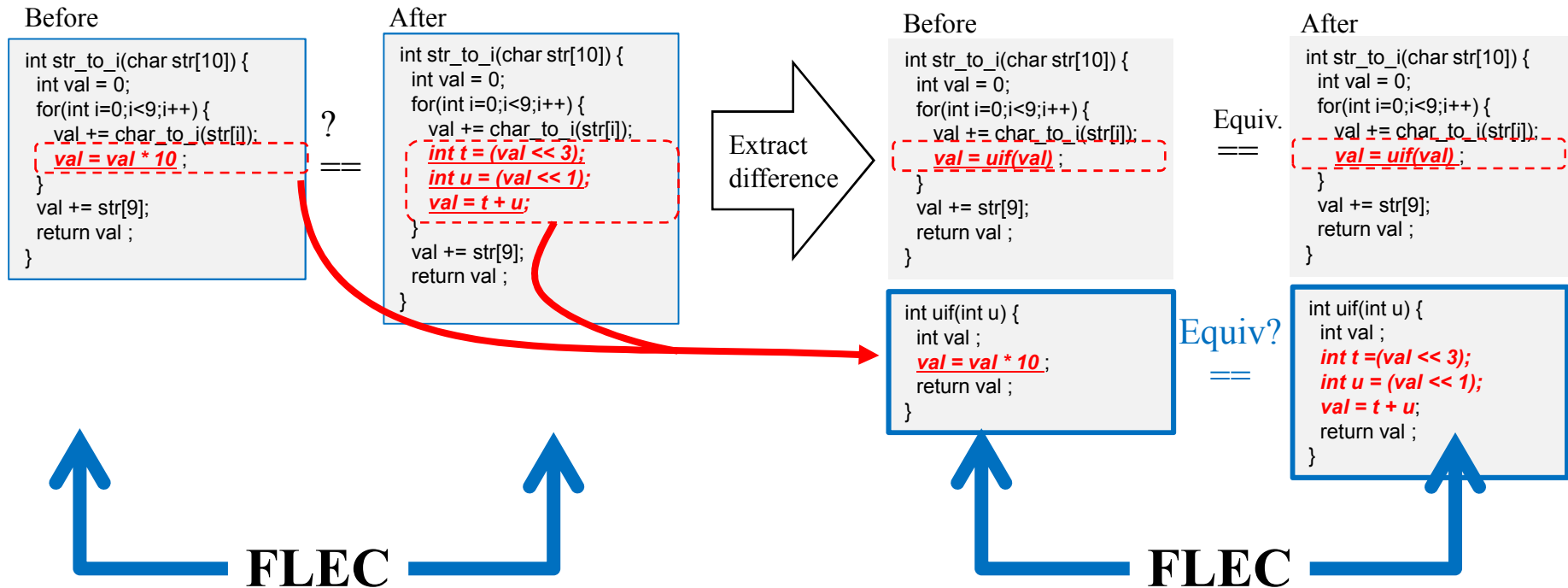


Extreme long verification time is required to guarantee the same correctness as the original code *even if using FLEC*

Difference-based Hierarchical Verification

Built a hierarchical verification framework for large C-descriptions and succeed to verify the design

- Extracting differences (code snippets) between designs
- Applying FLEC engine for the code snippets only



FLEC failed even after 3 days because the entire code verification is too large to be evaluated.

FLEC succeeded within several seconds because extracted snippets are more easily evaluated

Circuit & Architecture Technologies: Transient- & Permanent-Fault-Tolerant FPGA

■ Basic Idea:

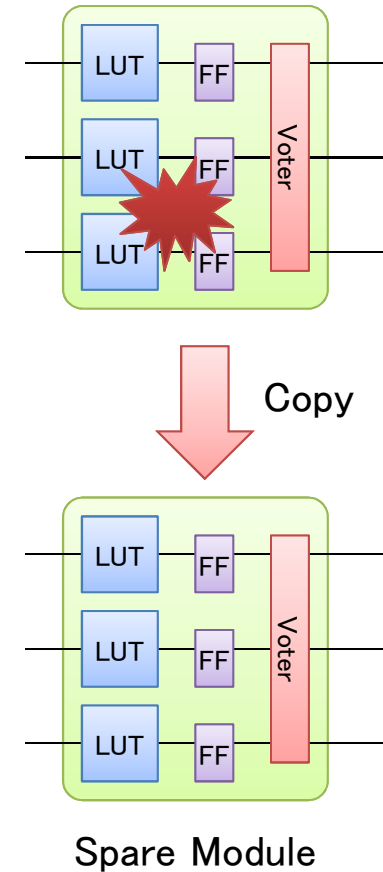
- ◆ Triple Modular Redundancy
 - to detect faults
- ◆ Dynamic Partial Reconfiguration
 - to replace faulty module with spare module

■ Goal : “One FPGA both for Normal and for Dependable Use”

- ◆ Minimizing hardware overhead esp. in normal use
 - Voters implemented as Hard-Wired Logic
 - Reconfiguration Controller implemented in User Logic

■ Non-Stop Dynamic Reconfiguration

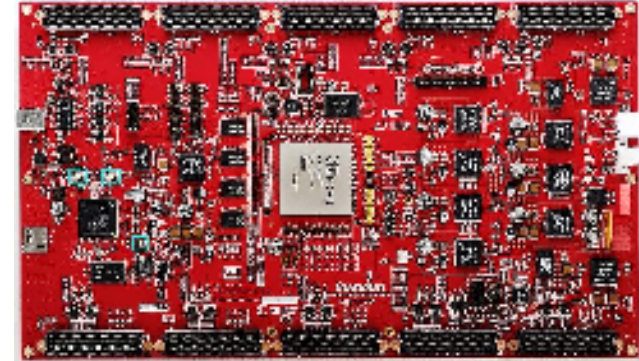
- ◆ when dynamically copy the contents of FFs from faulty module to spare module, the voter of another spare module is use to check successful completion



Circuit & Architecture Technologies: Timing-Fault-Tolerant Circuit & Processor

- Against Random Variation of LSIs

- ◆ Dynamic Timing Fault Detection & Recovery



FPGA Board for Demonstration

- Clocking Scheme Enabling Dynamic Time Borrowing

- ◆ Combination of 2-Phase Latch System + Timing Fault Detection
 - Clock Cycle is not determined by Worst- but by Typical-Case Delays
 - Doubles the Max Clk Frequency

- Timing-Fault-Tolerant Processor Architecture

- ◆ New Configuration of Store Buffer in Commitment Pipeline
 - Applicable to out-of-order superscalar processors

Circuit & Architecture Technologies: Plan to Yield Practical Applications

■ Fault-Tolerant FPGA

◆ Cooperation with ...

- Institute of Space and Astronautical Science (JAXA)
- NEC Space System Division / NEC Toshiba Space system
- Hitachi Research Laboratory

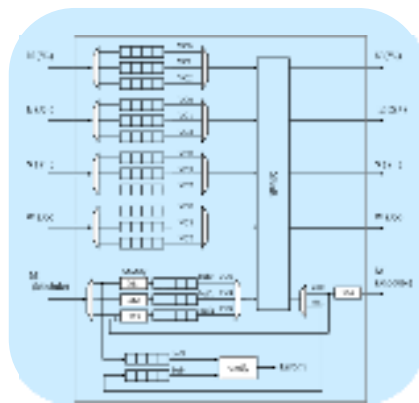
■ Timing-Fault-Tolerant Circuit & Processor

◆ Discussion with LSI vendors

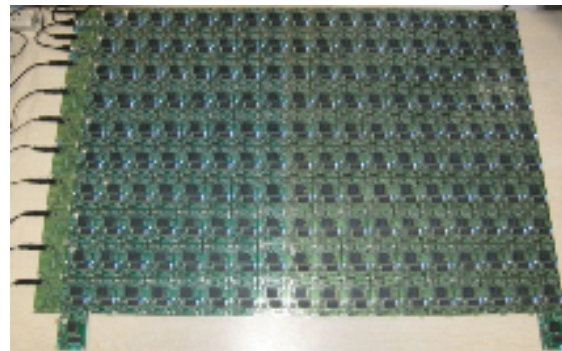
- Renesas
- Intel, AMD, ARM, etc... (plan)

Dependable and high performance many-core architecture ¹⁰

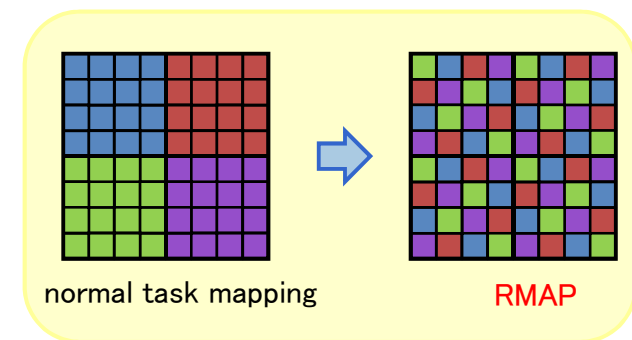
- Development of **on-chip multifunction routers** supporting ultra dependability
 - Designed multifunction router has 3 unique functions for Router-based DMR (Dual Modular Redundancy) and error detection
 - packet duplication
 - modification of packet destination
 - packet level error detection
- Development of **180 FPGA prototyping system**
 - With realistic configurations, our HW system emulating a many-core processor is **129x faster** than the SW simulator
 - Development and evaluations of our **task mapping method and the dependable mechanism** for a many-nodes system



Multifunction router



Many-core prototyping system



Task mapping method RMAP