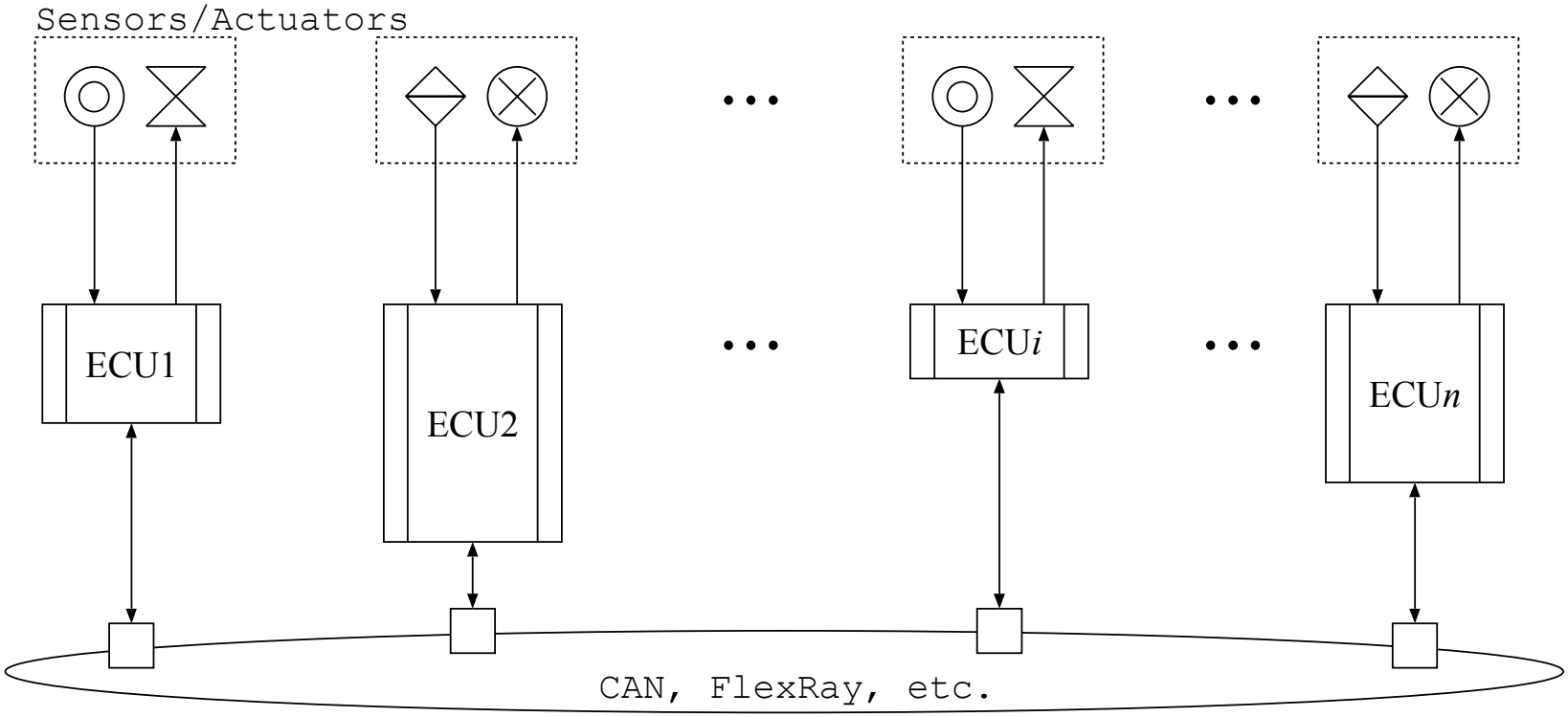
# Development of Dependable Network-on-Chip Platform

**Tomohiro Yoneda** (*National Institute of Informatics*)
**Masashi Imai** (*Hirosaki University*)
**Takahiro Hanyu** (*Tohoku University*)
**Hiroshi Saito** (*University of Aizu*)
**Kenji Kise** (*Tokyo Institute of Technology*)

National Institute of Informatics
国立情報学研究所

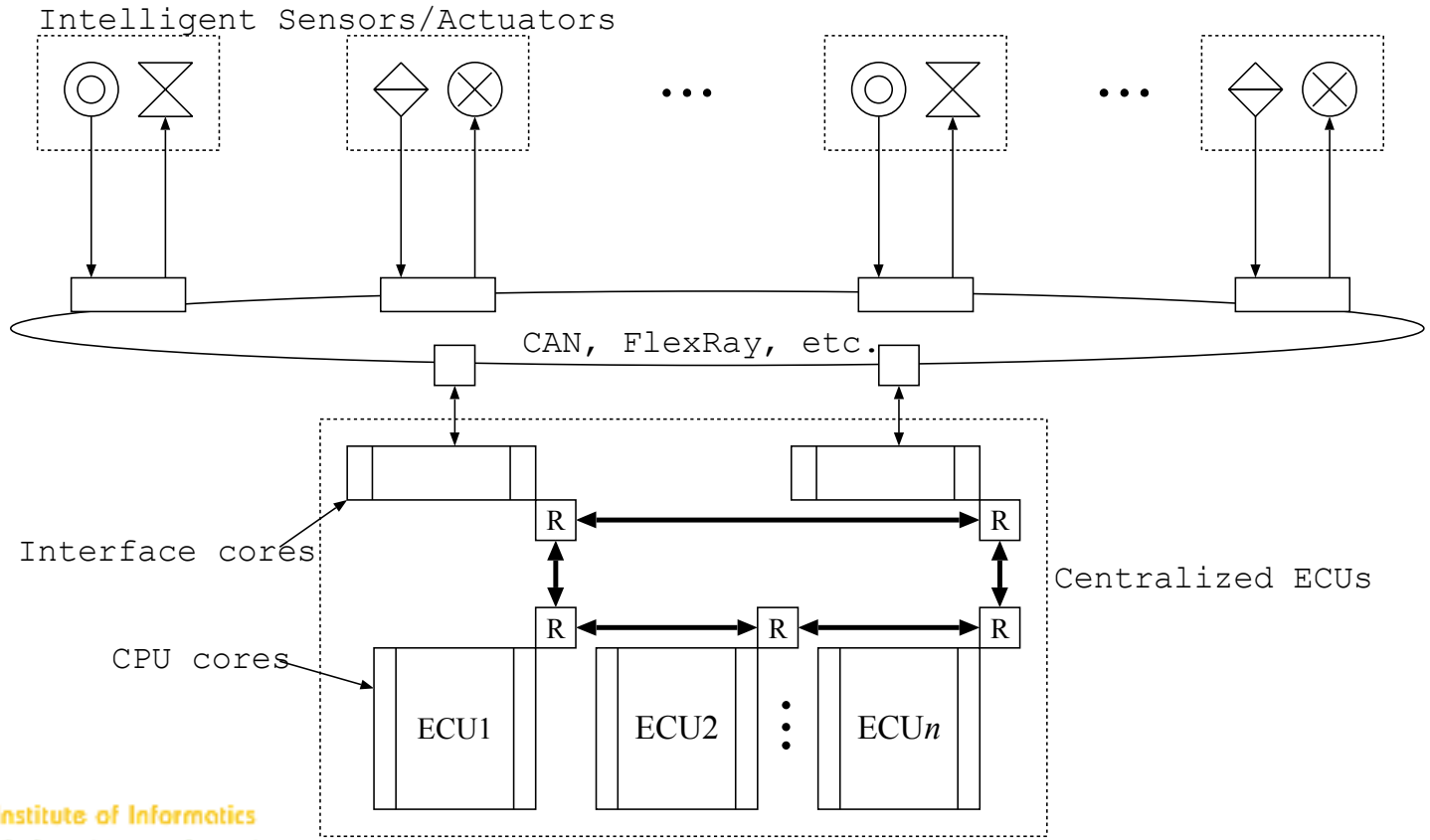
# Backgrounds

- Recent cars are equipped with many ECUs
  - Conventional ECU configuration



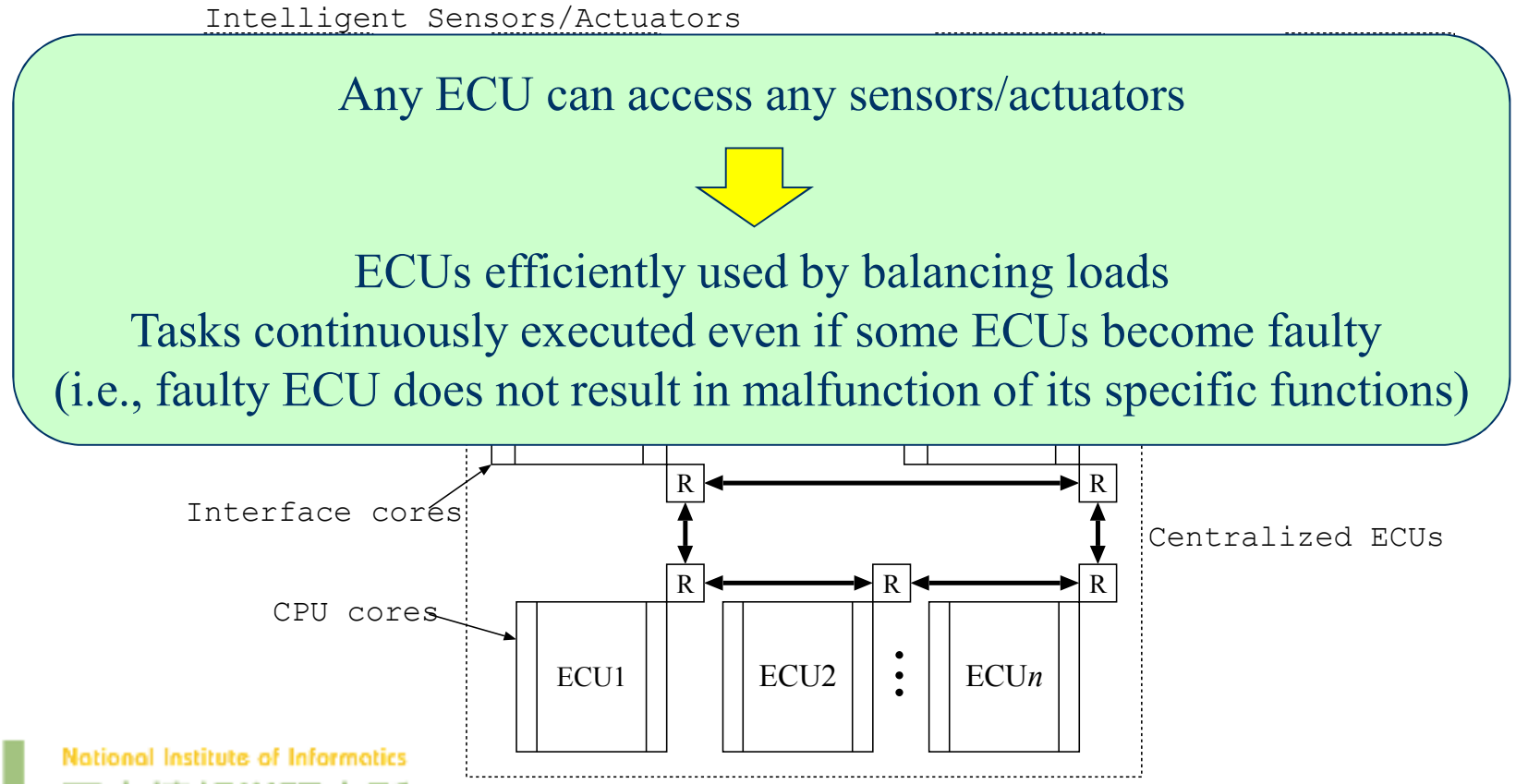
# Backgrounds

- Recent cars are equipped with many ECUs
  - Centralized ECU approach



# Backgrounds

- Recent cars are equipped with many ECUs
  - Centralized ECU approach

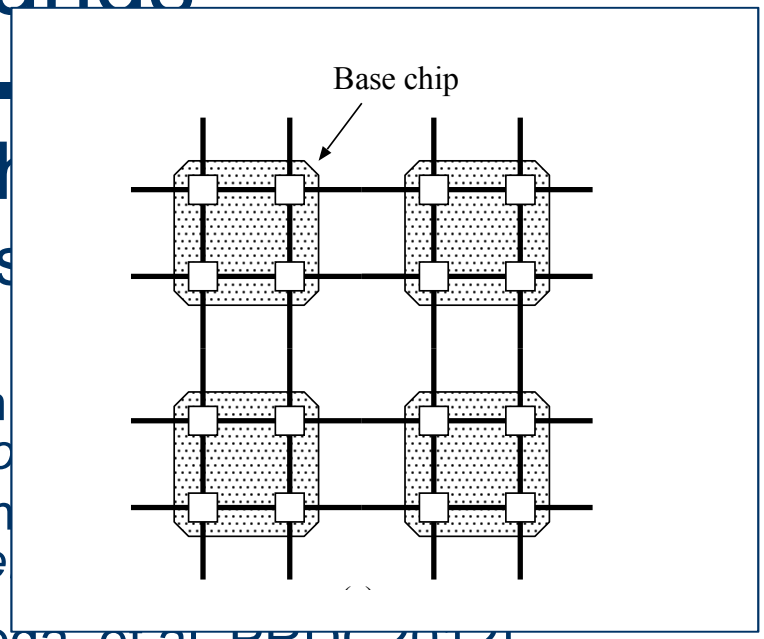


# Backgrounds

- Centralized ECU approach
  - NoC (Network-on-Chip) based
    - Some European projects
      - Recomp: Reduced certification costs for trusted multi-core platforms. *http://atc.ugr.es/recomp/.*
      - Race: Robust and reliant automotive computing environment for future ecars. *http://projekt-race.de/.*
  - Multi-Chip NoC based [Yoneda, et al. PRDC2012]
    - Multiple NoCs are connected via off-chip links
      - On-chip networks seamlessly extended to multi-chip networks
    - Advantages
      - Cost-effective : small NoC chips are cheap, and various sizes of configuration are possible (without developing different sizes of NoCs)
      - Chip-level redundancy : tolerate a chip fault

# Backgrounds

- Centralized ECU approach
  - NoC (Network-on-Chip) bas
    - Some European projects
      - Recomp: Reduced certification platforms. *http://atc.ugr.es/reco*
      - Race: Robust and reliant auton future ecars. *http://projekt-race*
  - Multi-Chip NoC based [Yoneda, et al. PRDC2012]
    - Multiple NoCs are connected via off-chip links
      - On-chip networks seamlessly extended to multi-chip networks
    - Advantages
      - Cost-effective : small NoC chips are cheap, and various sizes of configuration are possible (without developing different sizes of NoCs)
      - Chip-level redundancy : tolerate a chip fault



# Our Project

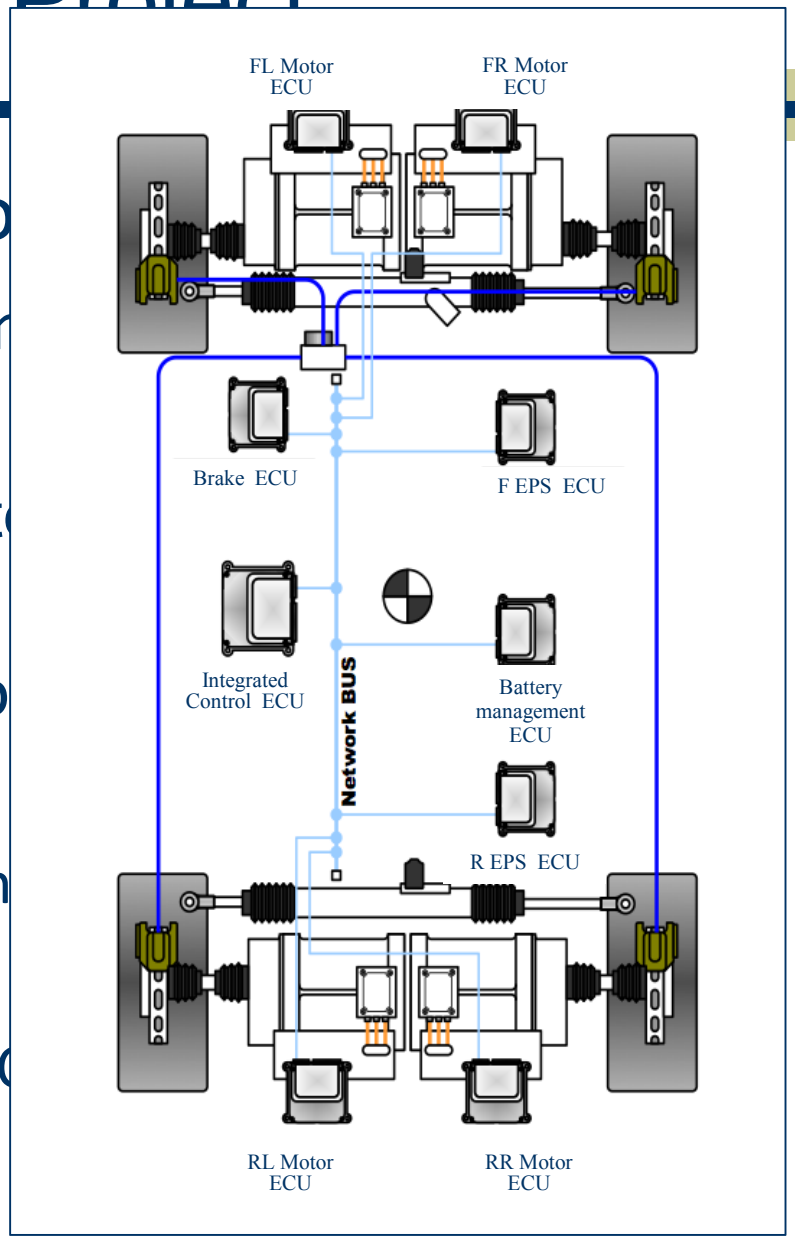
- Hardware platform
  - Multi-Chip NoC
    - Dependable, adaptive, deadlock-free routing
    - Efficient inter-chip communication technology
  - Evaluation board
- Task execution
  - Pair & Swap
  - SmartCore
- Task allocation
  - Redundant allocation, redundant scheduling

# Our Project

- Automotive Application
  - Integrated attitude control system for a four-wheel drive car
    - Torque, brake, and steering control of 4 wheels performed by ECUs
  - Highly cooperative process needed by each ECU
    - Integrated Control ECU
    - 2 Electric Power Steering Control ECUs
    - Brake Control ECU
    - Battery Management ECU

# Our Project

- Automotive Applicatio
  - Integrated attitude cor wheel drive car
    - Torque, brake, and st performed by ECUs
  - Highly cooperative pro
    - Integrated Control ECU
    - 2 Electric Power Steerin
    - Brake Control ECU
    - Battery Management E

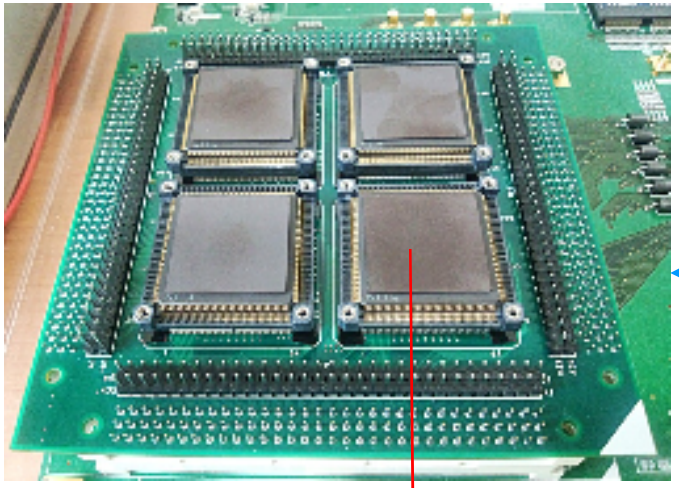


# Our Project

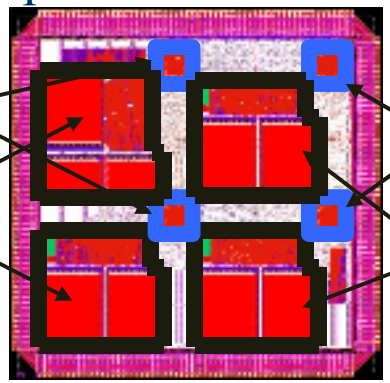
- Characteristics of this application
  - Stopping control is very dangerous
    - Higher availability is required

# Experimental system

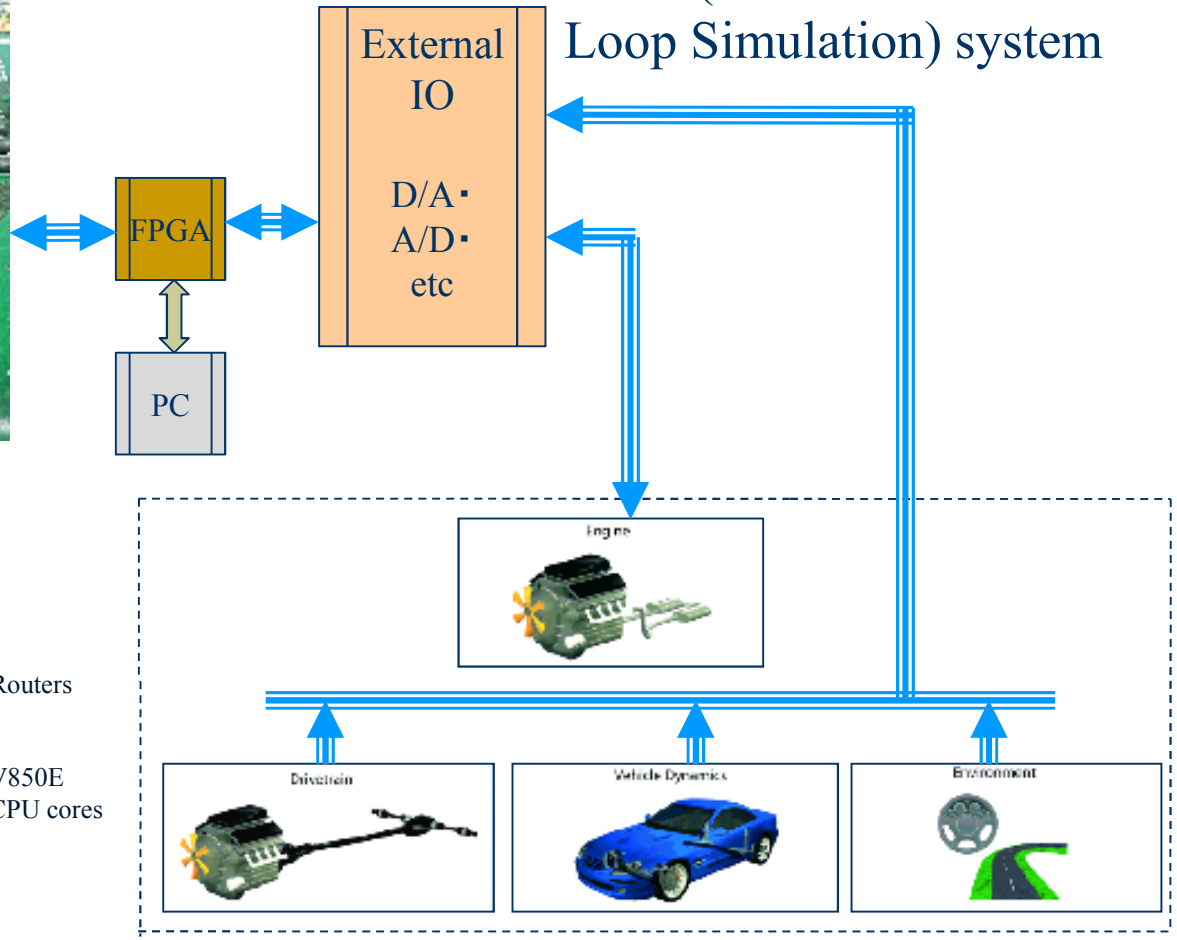
Base chip × 4



Base chip




HILS (Hardware In the Loop Simulation) system



# Ongoing work

- Evaluation kit
  - NoC implementation
    - 4 Multi-Chip ASICs
    - Vertex7(XC7VLX690T)
  - HILS interface
  - Pseudo HIL-plant models (executable on PC)
  - Redundant task allocation tool
    - Input: (Simplex) Simulink model for application
    - Output: Executable codes for redundant cores