Semiconductor

R&D Project Title :
Performance Balance Engineering for Hetero-integrate 3D CFET SRAM

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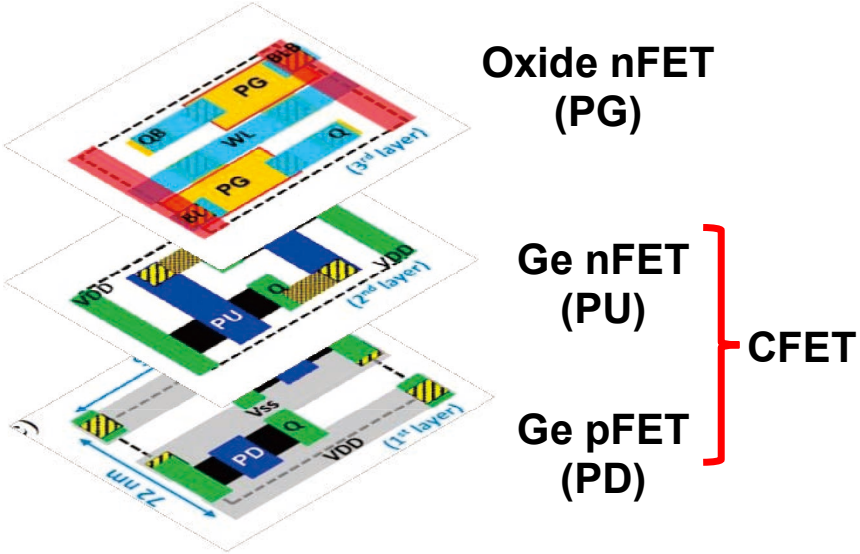
Summary :

This project focuses on realizing performance-balanced 3D CFET SRAM (low power consumption semiconductor memory) with extremely scaled cell size and low leakage current through multiple stacked hetero-integrated channel technology. The specific Design Technology Co-Optimization (DTCO) for 3D CFET SRAM can be conducted through TCAD (Technology Computer Aided Design) simulation.

The power consumption per bit cell of the designed 3D CFET SRAM is expected to reduce by 70 % compared to the 2 nm node SRAM cell, which contributes to reducing energy consumption in data centers, etc., leading to a carbon-neutralized society.



Hetero-integrate 3D CFET SRAM